EC8453 - LINEAR INTEGRATED CIRCUITS

COURSE OUTCOMES:

CO1. Apply knowledge of differential amplifiers, current sources in analyzing basic building blocks of operational amplifiers and understanding Characteristics of op amp.

CO2. Analyze and design linear and non-linear applications of operational amplifiers.

CO3. Understand the concept of analog multiplier and design analog circuits using PLL.

CO4. Explain the concept in different types of ADC and DAC.

CO5. Generate waveforms using OP – AMP Circuits.

CO6. Design special function ICs.

UNIT – I

BASICS OF OPERATIONAL AMPLIFIERS

Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations – JFET Operational Amplifiers– LF155 and TL082.

PART – A

1. Define an Integrated circuit. (Remember)

An integrated circuit(IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

2. Mention the advantages of integrated circuits over discrete components. (May 2010),[NOV/DEC 2013], [MAY/JUNE 2014][NOV/DEC 2014](Remember)

*Miniaturization and hence increased equipment density.
*Cost reduction due to batch processing.
*Increased system reliability due to the elimination of soldered joints.
*Improved functional performance.
*Matched devices. *Increased operating speeds.
*Reduction in power consumption.

3. Define sheet resistance. (Remember) (May 2010)

Sheet resistance is defined as the resistance in ohms /square offered by the diffused area.

4. What is the use of buried n+ layer in monolithic IC transistor? (Remember) (MAY2010)

The buried n+ layer provides a low resistance path in the active collector region for the flow of current

5. What are the two common methods for obtaining integrated capacitors? (Remember) (May 2010)

- Monolithic junction capacitor
- Thin-flim capacitor

6. What is active load? Where it is used and why? (Understand) (MAY/JUNE 2010)

The active load realized using current source in place of the passive load in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage.

7. Why open loop OP-AMP configurations are not used in linear Applications? (Understand) (May 2010)

The open loop gain of the op-amp is not a constant and it varies with changing the temperature and variations in power supply. Also the bandwidth of the open loop op-amp is negligibly small. For this reasons open loop OP-AMP configurations are not used in linear applications.

8. Define virtual ground of a OP-Amp? (Remember) (May/June 2010)

A virtual ground is a ground which acts like a ground. It is a point that is at the fixed ground potential (0v), though it is not practically connected to the actual ground or common terminal of the circuit.

9. Define input offset voltage. (Remember) [NOV/DEC 2013]

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage.

10. Define input offset current. State the reasons for the offset currents at the input of the op-amp. (Remember)

The difference between the bias currents at the input terminals of the op-amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents.

11. Define CMRR of an op-amp. (Remember) (DEC 09)

The relative sensitivity of an op-amp to a difference signal as compared to a common –mode signal is called the common –mode rejection ratio. It is expressed in decibels.

CMRR= Ad/Ac

12. What are the applications of current sources? (Remember)

Transistor current sources are widely used in analog ICs both as biasing elements and as load devices for amplifier stages.

13. What is the advantage of widlar current source over constant current source? (Understand)

Using constant current source output current of small magnitude(micro amp range) is not attainable due to the limitations in chip area. Widlar current source is useful for obtaining small output currents. Sensitivity of widlar current source is less compared to constant current source.

14. Mention the advantages of Wilson current source. (Remember)

(i) Provides high output resistance.

(ii) Offers low sensitivity to transistor base current

15. Define sensitivity (Remember)

Sensitivity is defined as the percentage or fractional change in output current per percentage or fractional change in power-supply voltage.

16. What are the limitations in a temperature compensated Zener-reference source? (Understand)

A power supply voltage of at least 7 to 10 V is required to place the diode in the breakdown region and that substantial noise is introduced in the circuit by the avalanching diode

17. In practical op-amps, what is the effect of high frequency on its performance?(Remember)

The open-loop gain of op-amp decreases at higher frequencies due to the presence of parasitic capacitance. The closed-loop gain increases at higher frequencies and leads to instability.

18. What is the need for frequency compensation in practical op-amps? (Remember)

Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability.

19. Define slew rate. (Remember) (MAY 2010), [MAY/JUNE 2014] [MAY/JUNE 2015]

The slew rate is defined as the maximum rate of change of output Voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage.

20. Why IC 741 is not used for high frequency applications? (Understand)

IC741 has a low slew rate because of the predominance of capacitance present in the circuit at higher frequencies. As frequency increases the output gets distorted due to limited slew rate.

21. What causes slew rate? (Understand) (DEC 09), [MAY/JUNE 2015][APR/MAY 2021]

There is a capacitor with-in or outside of an op-amp to prevent oscillation. The capacitor which prevents the output voltage from responding immediately to a fast changing input.

22. What happens when the common terminal of V+ and V- sources is not grounded? (DEC 09) (Understand)

If the common point of the two supplies is not grounded, twice the supply voltage will get applied and it may damage the op-amp.

23. What is an integrated circuit? (Remember) [APR/MAY 2010]

IC is a miniature low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.

24. What is current mirror?(Remember) [APR/MAY 2010]

A constant current source (current mirror) uses a transistor in the active mode of operation where the collector current is relatively independent of the collector voltage.

25. Define slew rate and CMRR. [NOV/DEC2010],[APR/MAY11]&[APR/MAY2013, APR/MAY2015] (Remember)

Slew rate is the maximum rate of change of output voltage caused by a step input voltage.

CMRR is defined as the ratio of differential mode gain to common mode gain.

26. Why are active loads preferred than passive loads in the input stage of an operational amplifier? (Understand) [NOV/DEC 2010]

A large value of resistance requires large chip area.

27. Name the different methods used in fabrication of integrated resistors. (Remember)

[APR/MAY 2011/ Nov / Dec 2012]

Diffused resistor, Epitaxial resistor, pinched resistor & Thin film resistor.

28. What are the two requirements to be met for a good current source? (Remember) [APR/MAY 2012]

Transistors should be matched in order to have same Vbe.

29. State the limitations of discrete circuits. (Remember) [APR/MAY 2013]

Operating speed is low due to parasitic capacitance effect.

Power consumption is more.

30. What is meant by monolithic IC? (Remember) [NOV/DEC 2014]

An integrated circuit or monolithic integrated circuit (also referred to as an IC, a chip, or a microchip) is a set of electronic circuits on one small plate ("chip") of semiconductor material, normally silicon.

31. What are the characteristics of an ideal op-amp? (Remember) [APR/MAY 2015] [APR/MAY 2017] [NOV/DEC 2018]

- Infinite open-loop gain G = V_{out} / 'v
- Infinite input impedance R_{in}, and so zero input current.
- Zero input offset voltage.
- Zero output impedance.
- Infinite bandwidth with zero phase shift and infinite slew rate.

32. A differential amplifier has a differential voltage gain of 2000 and common mode gain of 0.2. Determine CMRR in db. (Apply) [APR/MAY 2015]

CMRR= 20 LOG [2000/0.2] =80 dB

33. Mention two advantages of active load over passive load in an operational amplifier.

[**Nov / Dec 2015](Remember)**

34. Define input bias current and input offset current of an operational amplifier. [**Nov / Dec 2015] (Remember)**

Input Bias Current:

Ideally, no **current** flows into the **input** terminals of an **op amp**. In practice, there are always two **input bias** currents, IB+ and IB-

Input bias current I_B=$\frac{IB+ (-) IB-}{2}$

Input Offset Current:

One of the practical op –amp limitations that the input bias current for the two inputs may be slightly different. Even though the inputs are designed to be symmetrical, slight differences which occur in the manufacturing process may give slightly different bias currents. This offset current is typically on the order of a tenth of the input bias current, with 10nA being a representative offset current for a 741.

Input Offset Current I_{os}= |IB+ (-) IB-|

35. The output of an operational amplifier is 5V peak sine wave whose slew rate is 0.5V/μs. Find the maximum allowable frequency of the signal. [R (2008) Nov / Dec 2015]

(Apply)

fm =S/2πVm

Given S=0.5V/μs V_m=5V

fm=$0.5*10^{-6}/2\pi*5=1.59*10^{-08}$

36. Find the maximum frequency for sine wave output voltage 10V peak to Peak with an op-amp whose slew rate is 1V/μs. (Apply) [APR/MAY 2016]

fm =S/2πVm

Given S=1V/μs V_m=10V

fm=$1*10^{-6}/2\pi*10=1.59*10^{-08}$

37. Differentiate the ideal and practical characteristics of an op-amp. [APR/MAY 2016]

(Analyze)

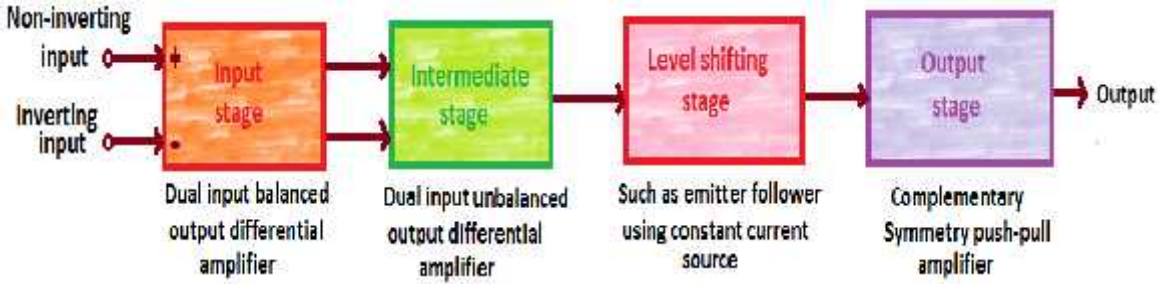
Ideal operational amplifier are characterized by

- Infinite gain
- Infinite input resistance
- Zero output resistance (order of 10's of ohms)
- Infinite bandwidth (practically restricted by slew rate)
- Linear irrespective of entire analog signal range No offsets and, so on.

Practical operational amplifier are characterized by

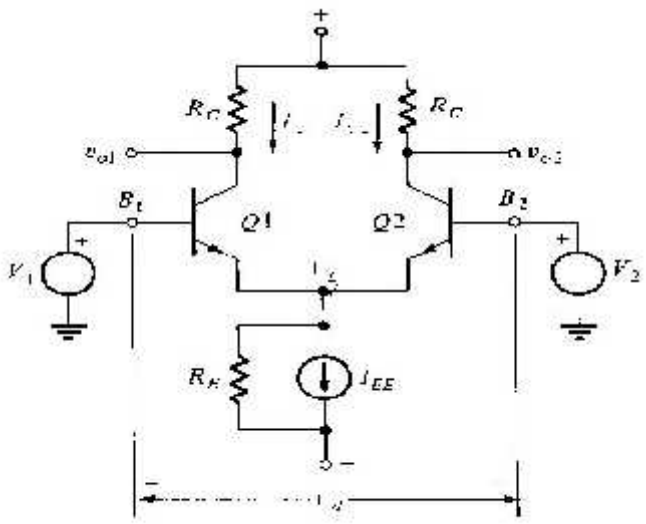
- Input resistance is of the of mega ohm Order due to differential stage at the front end
- Output resistance order of tens of ohms.
- Practically bandwidth of Opamp restricted by slew rate.

38) Draw the block diagram of general op-amp? (Nov/ Dec 2016) Remember

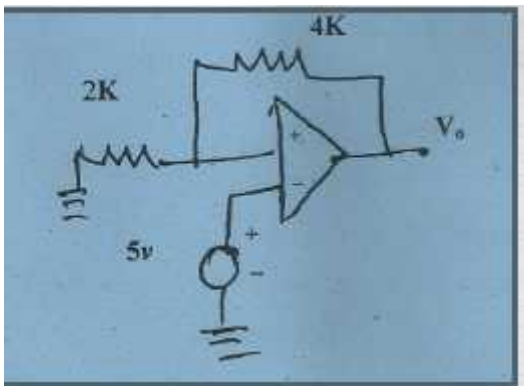


39) Draw the block diagram of symmetrical emitter coupled differential amplifier? (Nov/ Dec 2016) Remember

FIGURE 2-28
The emitter coupled or differential pair stage.



40) For the op amp shown in figure determine the voltage gain (Nov/ Dec 2016) (remember)

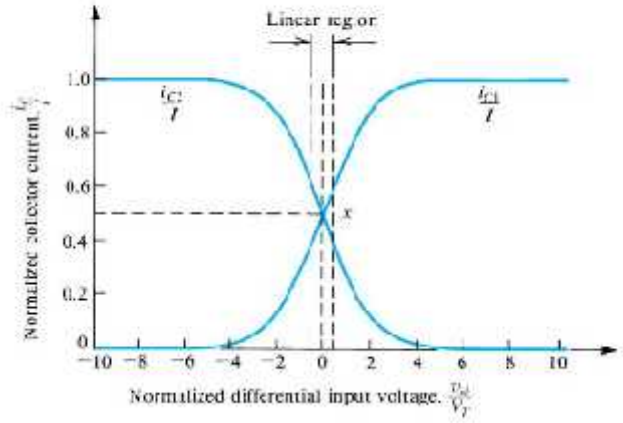


41) Why is the current mirror circuit used in differential amplifier stages (April /May 2017) (Understand)

The current mirror is a special case of constant current bias and the current mirror bias requires of constant current bias and therefore can be used to set up currents in differential amplifier stages. The current mirror bias requires fewer components than constant current bias circuits.

42. Draw the dc transfer characteristics of a BJt differential amplifier and define differential mode input voltages. [Nov /Dec 2017](Remember)

Differential Amplifier-Transfer Characteristics



43. The power supply rejection of an op-amp is 80dB for a lV change in supply voltage. Calculate the change in offset voltage. [Nov /Dec 2017] (Remember)

PSRR= Change in offset voltage/Change in supply voltage
= ΔVOS/ ΔVCC
ΔVOS = PSRR * ΔVCC = 0.1mV

44. Enumerate any two blocks associated with opamp block schematic. [Apr/May 2018](Remember)

- Dual input balanced output differential amplifier
- Dual input unbalanced output differential amplifier
- Level shifter
- Push-pull complementary amplifier

45.What are the two methods used to produce voltage sources[Apr/May 2018](Remember)

There are two methods which can be used to produce a voltage source,namely

1. Using an amplifier with negative feedback
2. Using the impedance transforming properties of transistor

46. Define Differential mode gain. (Nov/ Dec 2018) (remember)

Differential gain is the gain with which differential amplifier amplifies the difference between two input signals V1 and V2.It is denoted by A_d

$$A_d = V_0/V_d$$

47. What is the significance of current mirror circuit? [Apr/May 2019](Remember)

Constant current bias can be easily replaced by current mirror circuit to improve CMRR.

- Provides very high emitter resistance $R_{E.}$
- Requires les components than constant current bias.
- Simple to design.
- Easy to fabricate

48. Mention the applications of LF155. [Apr/May 2019](Remember)

Output amplifiers for D/A converters

Fast sample and Hold circuits

High speed integrators

Photocell Amplifiers

High input impedance buffers.

49. What are the assumptions made from ideal opamp characteristics? [Apr/May 2021](Remember)

- An ideal opamp draws no current at both input terminals because of infinite input impedance.
- Since gain is infinity,the voltage between the inverting and non inverting terminalsi.e the differential input voltage is ideally zero
- Since R0= 0,output can drive infinite number of other devices.

PART – B

1. Explain the method of improving CMRR. (Understand) (16)

2. (a) Write a note on Widlar biasing circuit. (4) (Remember) [Apr '11]

(b) Explain the various circuits used to provide constant current bias in a differential amplifier. (12) (Understand)

3. Explain the method of improving the CMRR using active load. (16) (Understand) [May'03]

4. Explain the operation of differential amplifier and give its differential gain, common mode gain and CMRR. (Understand) (16)

5. Draw and explain the basic band gap reference circuit. (Understand) (16)

6. Derive the slew rate equation for an op-amp. (16) (Apply) [Nov'02]

7. Explain in detail about the frequency compensation applied to operational amplifiers. (Understand)

8. (a) Explain the method of improving the slew rate of an op-amp. (12) (Understand)

(b) Draw and explain briefly the equivalent circuit of an op-amp. (Understand) (4)

9. Draw and explain the internal block diagram of an op-amp. (16) (Understand) [Apr/May 2019**]** [Nov /Dec 2017]

10. Define and explain slew rate. What is full-power bandwidth? Also explain the methods adopted to improve slew rate [10] (Understand) [Apr'11]

11. Define output off-set voltage. Explain methods of nullify offset voltage (6) (Understand) [Apr '11]

12. (i) Define CMRR. Draw the circuit of an Op-amp differential amplifier and give the expression for CMRR. (8) (Apply)

(ii) Define Slew Rate. Explain the cause of slew rate and derive an expression for Slew rate for an op-amp voltage follower. (8) (Apply) [APR/MAY 2010] [NOV/DEC 2018]

13. Draw the circuit diagram of the output stage of the IC 741 OP AMP and explain its operation with clearly indicating the protection mechanisms indicated. (Apply) [NOV/DEC 2010]

14. With neat circuit diagram explain the operation of [MAY/JUN 2012]

(i) Voltage reference circuit using temperature compensation

(ii) Voltage reference circuit using avalanche diode reference (Understand)

16. (i) List and explain the non-ideal DC characteristics of an operational amplifier.(Understand)

[NOV/DEC 2014], [APR/MAY 2015] [Apr/May 2019]

(ii) Explain the AC characteristics of an operational amplifier [MAY/JUN 2012], [NOV/DEC 2014] [Apr/May 2019] (Understand)

17. Compare different configurations of Differential Amplifier. (Analyze) [May/June 2013]

18. For a dual input, balanced output differential amplifier, Rc = 2.2kΩ, Re =4.7kΩ, Rs1 = Rs2 = 50 Ω. The supply voltages are $\pm$ 10V. The hfe for the transistor is 50. Assume silicon transistors and hie = 1.4kΩ. Determine the operating point values, differential gain common mode gain and CMRR. (Apply) [May/June 2013]

19. State the advantages of Integrated circuits over discrete components.[May/June 2013] (Understand)

20. Explain the working of BJT Differential Amplifier with Active Load. (Understand) [NOV/DEC 2013] [NOV/DEC 2018]

21. Write down the characteristics and respective values of an ideal operational amplifier. (Understand) [NOV/DEC2 013]

22. Explain the internal circuit diagrams of IC 741.Discuss its AC and DC performance Characteristics. (Understand) [MAY/JUNE 2014]

23. With simple schematic of differential amplifier explain the function of operational amplifier? (8) (Understand) [APR/MAY 2015]

24. With the neat diagram, explain the input side of the internal circuit diagram of IC741. (16). (Apply) [Nov / Dec 2015]

25. What is the need for the frequency compensation in an OPAMP? With a suitable illustration, explain the pole-zero frequency compensation technique. (16) (Understand) [Nov / Dec 2015]

26. Draw the circuit diagram of a basic current mirror and explain its operation (8) (Analyze)[R (2008) Nov / Dec 2015] (Nov Dec 2016)

27. With a schematic diagram, explain the effect of R_E on CMRR in differential amplifier.(4) [APR/MAY 2016] (Analyze)

28. Discuss about the methods of improve the CMRR.(12). (Analyze) [APR/MAY 2016]

29) Explain the significance of virtual ground in an opamp. (Nov Dec 2016) (understand)

30) With diagram explain the operation of an inverting amplifier in closed loop configuration. Obtain the expression for closed loop gain (Nov Dec 2016) (Remember)

31) Assuming a slew rate for 741 IC is 0.5 tilp s. What is the maximum undistorted sine wave that can be obtained for 12 v peak. (Nov Dec 2016) (Apply)

32) Compare the features of ideal and practical opamp circuit ? (Nov Dec 2016) (understand)

33) A differential amplifier has CMRR = 1000. Differential inputs V 1= 1100 and V2=900 u V calculate the difference in output voltage if the differential gain Ad= 25000 (Nov Dec 2016) (Analyze)

34) Derive the functional parameters for an Inverting mode negative feedback gain circuit with a 741 OpAmp in IC Inverting mode, with R1= 1 Kohm, Rf 40 Kohm and Compute Af; Rif; Rof; BW; offset voltage. (April / May 2017) (Analyze)

35) Discuss briefly on the differential mode Instrumentation amplifier. (April / May 2017) (Remember)

36) What is input and output voltage and current offsets? How are they compensated? (April / May 2017) (Remember)

37) With neat diagram derive the AC performance close loop characteristics of OpAmp to discuss on the circuit Bandwidth, Frequency response and slewrate: (April / May 2017) (Remember)

38) Draw the transfer characteristics of an operational amplifier and explain the linear and non-linear operation. [Nov /Dec 2017] (understand)

39) Draw the inverting and non-inverting amplifier circuits of an op-amp in closed-loop configuration. Obtain the expressions for the closed-loopgain in these circuits. [Nov /Dec 2017] (understand)

40)Perform the AC analysis of the operational amplifier 741. [Nov /Dec 2017](understand)

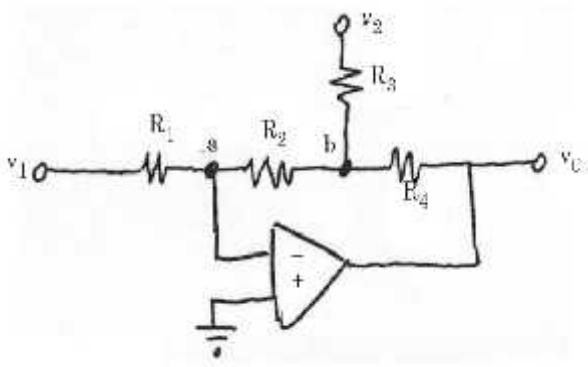
41) Discuss about the principle of operation differential amplifier using BJT[Apr/May 2018] (understand)

42)Explain about ideal opamp in detail with suitable diagram. [Apr/May 2018] (understand)

43)Draw the transfer characteristics of an operational amplifier and explain its linear and non-linear operation. [Nov /Dec 2018](understand)

44) Suppose that an amplifier with input resistance of 500KΩ or greater is needed and a voltage gain of -45).The feedback resistors are to be implemented in integrated form and have values of 10 KΩ. or less to conserve chip area.Choose a suitable configuration and specify the resistance values.Finally, estimate the resistor toleranceneeded so that the gain magnitude maintained within 5% of its nominal values. [APR/MAY 2019](Analyze)

46) For the circuit shown, Find V_0 as a function of V_1 and V_2**.[APR/MAY2021](Analyze)**



47) With neat sketch explain in detail the working of Widlar and Wilson current sources?
[APR/MAY2021](understand)

ASSIGNMENT QUESTIONS

1. For the DC level shifter shown in Fig 1, Determine the level shift between input and output voltages. (PO1)(REMEMBER)

2. Obtain the level shift Vo for the circuit shown in Fig. 2. (PO1)(REMEMBER)

3. A differential Amplifier has i) CMRR=1000 and ii)CMRR = 10,000.The first set of inputs is V1=100μV and V2=-100μV.The second set of input is V1=1100μV and V2= 900μV.Calculate the percentage difference in output voltage obtained for the two sets of input voltages and also comment on this. (PO2)(ANALYZE)

4. Design a i) constant current source ii) Widlar current source for generating a constant current of Io=10μA.Assume Vcc=10V, Vbe=0.7 V, β=125, V_T=25Mv.Find R1.Justify which circuit can be used for generating small current? (PO2) (PO3)(ANALYZE &CREATE)

5. Design a differential Amplifier for a differential gain of 5000 and CMRR 100.If the inputs are 290μV and 250 μV, Find the output voltage. (PO3)(CREATE)

6. An operational amplifier has a slew rate of 2V/μs. If the peak output is 15 V, What is the power bandwidth? (PO1) (REMEMBER)

7, An operational amplifier has a slew rate of 35V/μs. How long will it take for the output to change from 0 to 15V? (PO1) (REMEMBER)

8.The output of an opamp voltage follower is a triangular wave for a square wave input of frequency 2MHz and 8Vpp amplitude. What is the slew rate of opamp? (PO1) (REMEMBER)

9. Design a simple current source to provide an output current of 150μA.Assume Vcc=5V,Vbe=0.6 V, β=125. (PO3) (CREATE)

10.A peak to peak input signal of 400mV has to produce a peak to peak undistorted output voltage of 3V with a rise time of 4μs.Can IC741 be used for such application.? Justify. (PO1)

UNIT – II

APPLICATIONS OF OPERATIONAL AMPLIFIERS

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters..

PART - A

1. **Mention some of the linear applications of op – amps. (Remember) (DEC 09)**

Adder, subtractor, voltage –to- current converter, current –to- voltage converters, instrumentation amplifier, analog computation, power amplifier, etc are some of the linear op amp circuits.

2. Mention some of the non – linear applications of op-amps (Remember)

Rectifier, peak detector, clipper, clamper, sample and hold circuit, log amplifier, anti –log amplifier, multiplier are some of the non – linear op-amp circuits.

3. What are the areas of application of non-linear op- amp circuits? (Remember)

1. Industrial instrumentation
2. Communication
3. Signal processing

4. What is voltage follower? (Remember) (MAY 2010)[MAY/JUNE 2014]

A circuit in which output follows the input is called voltage follower.

5. What is the need for an instrumentation amplifier? (Remember)

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

6. List the features of instrumentation amplifier: (Remember)

1. High gain accuracy
2. High CMRR
3. High gain stability with low temperature co-efficient
4. Low dc offset
5. Low output impedance

7. What are the applications of V-I converter? (Remember)

1. Low voltage dc and ac voltmeter
2. LED
3. Zener diode tester

8. Define Band pass filter. (Remember) (MAY 2010)

The band pass filter is the combination of high and low pass filters, and this allows a specified range of frequencies to pass through.

9. Write transfer function of op amp as an integer. (Remember) [MAY 2010]

The transfer function of the integer is IAI=1/WR1cf

10. What do you mean by a precision rectifier? (Remember) [APR/MAY 2015]

The major limitation of ordinary diode is that it cannot rectify voltages below the cut – in voltage of the diode. A circuit designed by placing a diode in the feedback loop of an op – amp is called the precision diode and it is capable of rectifying input signals of the order of millivolt.

11. Write down the applications of precision diode. **(Remember)**

1. Half - wave rectifier
2. Full - Wave rectifier
3. Peak – value detector
4. Clipper
5. Clamper

12. Define Logarithmic and antilogarithmic amplifier. (Remember) (MAY 2010)

When a logarithmic PN junction is used in the feedback network of op-amp, the circuit exhibits log or antilog response. The logarithmic amplifier is a current to voltage converter with the transfer characteristics v0=vi In(If/Ii) Antilog amplifier is a decoding circuit which converts the logarithmically encoded signal back to the original signal levels as given by vl=vR10-kvi

13. Differentiate Schmitt trigger and comparator. (Remember) (MAY 2010)

Comparator.

1.It compares the input signal with references voltage then yields the output voltage . comparator output need not to be square wave

2. It need not consist of feedback

Schmitt trigger

1. It operates between two reference points namely UTP&LTP.
2. It employs positive feedback
3. Its output is square wave.

14. List the applications of Log amplifiers: (Remember)

1. Analog computation may require functions such as lnx, log x, sin hx etc. These functions can be performed by log amplifiers

2. Log amplifier can perform direct dB display on digital voltmeter and spectrum analyzer

3. Log amplifier can be used to compress the dynamic range of a signal

4. Comparator output need not to be square wave

15. Write down the condition for good differentiation. (Remember)

1.For good differentiation, the time period of the input signal must be greater than or equal to Rf C1

2. T> =R f C1 Where, R_f is the feedback resistance

3. C f is the input capacitance

16. What is a comparator? (Remember) (MAY 2010)

A comparator is a circuit which compares a signal voltage applied at one input of an op amp with a known reference voltage at the other input. It is an open loop op - amp with output +Vsat.

17. What are the applications of comparator? (Remember)

1. Zero crossing detectors

2. Window detector

3. Time marker generator

4. Phase detector

18. What is a Schmitt trigger? (Remember) (DEC 09, MAY 10)

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform.

19. What is a Schmitt trigger? (Remember) (DEC 09, MAY 10)

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages,

20. Which are the reference voltages of the input waveform? (Remember)

i. RC phase shift oscillator

ii. Wein bridge oscillator

21. What are the characteristics of a comparator? (Remember) [APR/MAY 2015]

1. Speed of operation

2. Accuracy

3. Compatibility of the output

22. What is a filter? (Remember)

Filter is a frequency selective circuit that passes signal of specified band of frequencies and attenuates the signals of frequencies outside the band

23. What are the demerits of passive filters? (Remember)

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive. For low frequency applications, more number of

turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation.

24. What are the advantages of active filters? (Remember)

Active filters used op- amp as the active element and resistors and capacitors as passive elements.

25. Give the schematic of op-amp based current to voltage converter. [APR/MAY 2010](Apply)

26. Draw the circuit diagram of differentiator and give its output equation [APR/MAY 10] (Apply)

27. Compare the performance of inverting and non-inverting operational amplifier configurations.(Analyze) [NOV/DEC 2010]

Inverting Amplifier:

Gain = -Rf / Ri Input resistance = Ri

Non Inverting Amplifier:

Gain = 1+Rf / Ri Input resistance = Very large (∞)

28. Why is frequency compensation required in operational amplifier? [NOV/DEC 2010] (Understand)

To improve Stability of the circuit.

29. How do the precision rectifiers differ from the conventional rectifier [APR/MAY 2011] [NOV/DEC 2014], [APR/MAY 2015] (Understand)

To rectify voltage below the cut in voltage (0.7V) of a diode.

30. What are the important features of an instrumentation amplifier [APR/MAY 2011] (Remember)

High gain accuracy, High CMRR, Low DC offset & low output impedance.

31. What is comparator? (Remember) [APR/MAY 2012]

It is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference at other input.

32. Give an application of an Inverting Amplifier. (Remember) [May / June 2013]

Scale changer, inverting summer.

33. Draw and write equation of an integrator using an op-amp. (Remember) [NOV/DEC 2010]

$$V0(t) = \frac{-1}{R1Cf}\int_0^t Vi(t)dt + V0(0)$$

34. Give one application of voltage follower, Schmitt Trigger, Clamper and Peak Detector. (Remember) [NOV/DEC 2013]

Voltage follower- Buffer
Schmitt Trigger – Squarer circuit
Clamper – Analog TV receivers
Peak Detector – AM communication

35. Define Bandwidth of a filter? (Remember) [NOV/DEC 2014]

Bandwidth is the difference between the upper and lower cutoff frequencies.

36. What is Hysteresis and mention the purpose of hysteresis in a comparator.

(Remember) [APR/MAY 2015].

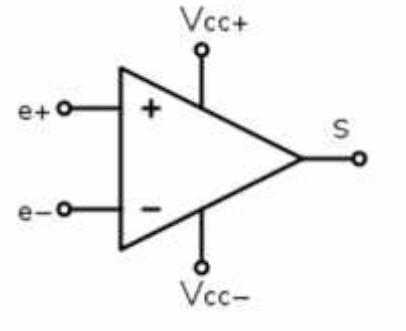
The difference between upper and lower threshold voltages in a comparator is called hysteresis. The voltage span of hysteresis is set to be greater than the peak to peak noise voltage**.** Therefore there will not be any incorrect variations due to noise signals.

37. Determine the output voltage for the circuit shown in figure 1 when [Nov / Dec 2015]

(Apply)

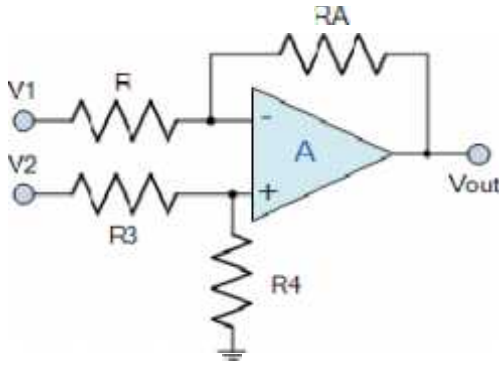
a.Vin=-2V and

b.Vin=3V Given V_{cc}=+-10V e+=1.5 e - =V_{in}



38. Design and sketch an operational amplifier subtractor circuit. (Analyze)

[R (2008) Nov / Dec 2015]

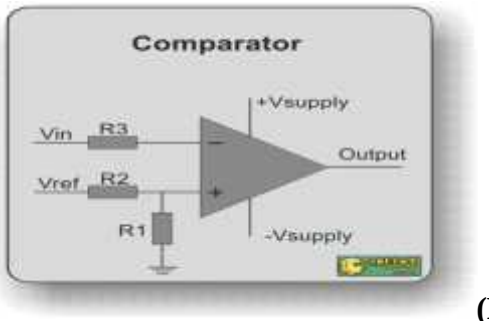


$$V_{out} = -\frac{RA}{R}(V2 - V1)$$

39. What is the difference between basic comparator and Schmitt trigger? (Remember) [R (2008) Nov / Dec 2015]

In electronics, a **Schmitt trigger** is a **comparator** circuit **with** hysteresis implemented by applying positive feedback to the noninverting input of a **comparator or** differential **amplifier**. ... In the non-inverting configuration, when the input is higher than a chosen threshold, the output is high.

40. Draw the circuit diagram of a comparator. Mention its applications. [APR/MAY 2016]

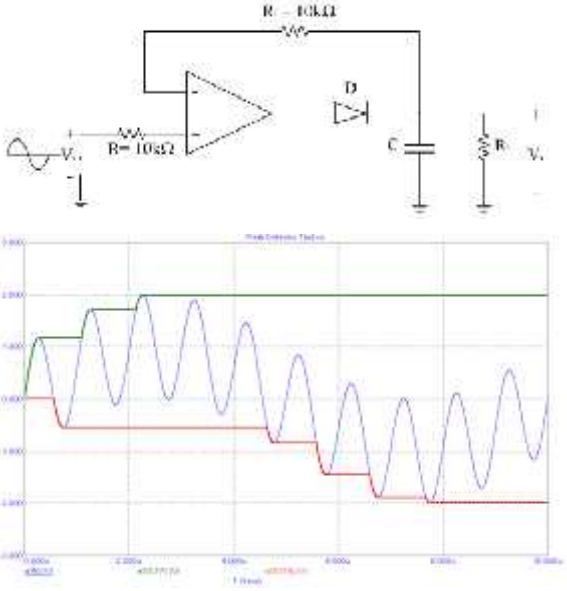


(Remember)

Applications of Comparator:

Threshold Detector, Zero Crossing Detector and Schmitt Trigger

41) Draw the circuit diagram of a peak detector with waveforms (Nov /Dec 2016) (Remember)



42) What is the need for converting a First order Filter into a Second order filter? (April May 2017) (Understand)

In order to get the sharp attenuation at the stop band we are converting a first order filter to a second order filter.

43) How is the current characteristic of a PN junction employed in a Log Amplifier ? (April May 2017) (Understand)

The analysis is the same as above for the trans diode connection, but the logarithmic range is limited to four or five decades because the base current adds to the collector current.The circuit polarity can be easily changed by reversing the transistor, the stability improves, and the response is faster.

44) How are square root and square of a signal obtained with multiplier circuit ? (April May 2017) (Understand)

To use a multiplier to square a voltage simply connect that voltage to both inputs. Connect your input voltage to opamp's non-inverting input, the opamp output to the multiply inputs and the multiply output to opamp's inverting input.

45) State the limitations of an ideal integrator. (Remember) [**Nov / Dec 2017]**

Drawbacks in ideal integrator:

1. Bandwidth is very small and used for only small range of input frequencies.
2. For dc input (f = 0), reactance of capacitance, Xc is infinite. Because of this op-amp goes into open loop configuration.In open loop configuration the gain is infinite and hence the small input offset voltages are also amplified and appears at output as error.

46) How will you realize a peak detector using a precision rectifier ? (Remember) [**Nov / Dec 2017]**

A capacitor is added at the output of the precision rectifier.The circuit follows the voltage peas of a signaland stores the highest value on the capacitor.

47) What is the function of phase shift circuit? [Apr/May 2018] (Remember)

A phase shift circuit is one in which all signals are transmitted from input to output without change in amplitude but change in circuit introduces a phase shift as signal transmits from input to output.

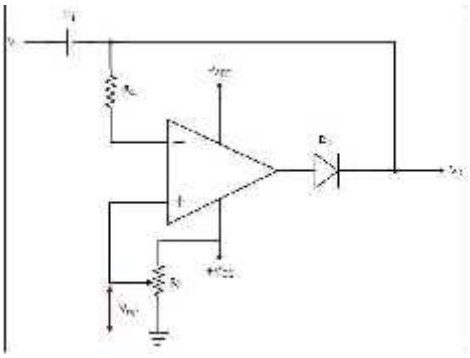
48) Write the other name of clipper circuit? [Apr/May 2018] (Remember)

Clipper circuit is also called as Limiter circuit.

49) How does operational amplifier work as an integrator? [**Nov / Dec 2018] (Remember)**

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator.Such circuit is obtained by using a basic inverting amplifier configuration with the feedback resistor R_f replaced by a capacitor.

50) Draw the circuit of a clipper using opamp? [**Nov / Dec 2018] (Remember)**



51) How does a zero crossing detector work? [Apr/May 2019](Remember)

Zero crossing detector is also known as sine wave to square wave converter.Comparator can be used as a zero crossing detector by setting V_{ref} to zero and applying sinusoidal signal as input.

52. What is the need for an integrator? [Apr/May 2021](Remember)

The gain of differentiator increases linearly with frequency and it tends to amplifylow frequency noise,which may result in spurious oscillations,integrators are preferred over differentiators.

PART - B

1. Design a Second order Butterworth LPF having a upper cutoff frequency of 1 KHz. .**[APR/MAY2021] (Analyze)**

2. Design a square wave oscillator for f_0 = 1 KHz using 741 op-amp and a DC supply voltage of +/-12V. (Analyze)

3. a) Discuss the working of instrumentation amplifier . Name two applications of the same. (10) (Understand) .**[APR/MAY2021]** [May'06]

4. Discuss in detail the working of a RC phase shift oscillator. (Understand)

5. Design Wien Bridge oscillator of 1 KHz frequency. (Analyze)

6. Design an op – amp Schmitt trigger with VUT= 2V, VLT= -4V & the output swings b/w +10V. If the i /p is 5 sin wt, plot i/p & o/p waveforms. (Analyze)

7. a) Compare the RC phase shift and Wien bridge oscillator. (Analyze) (8)

b) Design a RC phase shift oscillator and a Wien bridge oscillator of frequency 1 KHz. (Assume C= 0.01 μF). (8) (Analyze) [Nov'05]

8. With diagram explain the operation of inverting and non-inverting amplifier. (Apply)

9. Draw the circuit diagram of a second order Butterworth active LPF and derive its transfer function. (Apply) [ECE Jun'07]

10. Draw an instrumentation amplifier whose gain is controlled by adjustable gain and explain its Working concept. (Apply) [EEE May'08]

11. Explain the circuit operation of logarithmic amplifier with two op-amps. [EEE May'08] (Understand)

12. With neat circuit, explain the operation of Schmitt trigger. (Understand) [ECE May'08]

13. Explain about positive and negative clipper. (Understand)

14. Explain about zero crossing detector and peak detector. (Understand)

15. With the help of circuits and necessary equations, explain how log and antilog computations are performed using IC741. (Analyze) [Apr '11]

16. Explain the operation of the following op-amp applications. [Apr '11]

1. Scale Changer (4)
2. Voltage follower (4)
3. Non-Inverting adder (4)
4. Integrator (4) (Understand)

17. (i) Design a first order Low-pass filter for cut-off frequency of 2 KHz and pass-band gain of 2. (8) (Analyze) [APR/MAY 2010]

(ii) Explain a positive clipper circuit using an Op-amp and a diode with neat diagrams . (Understand)

18. (i) Design a circuit to implement $V_0=0.545V_3+ 0.273V_4-1.25V_1-2V_2$.[APR/MAY 2010] (Analyze)

(ii) Draw and explain a simple Op-amp differentiator. Mention its limitations. Explain with a neat diagram how it can be overcome in a practical differentiator. Design an Op-amp differentiator that will differentiate an input signal with maximum frequency f max =100Hz. (Analyze)

19. With relevant circuits, explain the following applications of OPAMP. [NOV/DEC 2010]

(i) Voltage to current converters
(ii) Multiplier (Understand)

20. (i) Explain the steps involved in the design of a band pass filter using OPAMP.
(ii) Write a note on Schmitt trigger. [NOV/DEC 2010]
(Understand)

21 (i).Sketch the basic circuit using op amp to perform the mathematical operation of differentiation and explain? What are the limitations of an ordinary op-amp differentiator? Draw and explain the operation of a practical differentiator that will eliminate the limitations. (Analyze)

(ii) Draw and explain the circuit of a voltage to current convertor if the load is

(1) Floating (2) Grounded (Understand) [MAY/JUN 2012][APR/MAY 2018]

22. (i) Explain the working of OP-AMP based Schmitt trigger circuit. (Understand)

[MAY/JUN 2012] [APR/MAY 2015] [APR/MAY 2019]

(ii)Design OP-AMP based second order active low pass filter with cut off frequency 2 kHz. (Analyze)

23. a) i) What do you understand by an Instrumentation Amplifier?(Remember)

ii) State the requirements of a good Instrumentation Amplifier. (Remember)

iii) Draw the circuit diagram and explain the working of Instrumentation Amplifier. (Understand)

iv) Mention the specific advantages of three op-amp Instrumentation Amplifier circuit.

(Remember) [May / June 2013]

24. i) What do you understand by an Integrator? (Understand)

ii) Draw and explain an ideal active op-amp Integrator circuit. (Understand)

iii) Draw the I/O waveforms for integrator (Apply)

1) Step input signal.
2) Square wave input signal
3) Sine wave input signal.

Derive the expression for change in output voltage. (Apply)

i) List the applications of practical Integrator. (Remember)

ii) Design a practical integrator circuit with a dc gain of 10, to integrate a square wave of 10 KHz. (Analyze) [May / June 2013]

25. Explain the working of i) Instrumentation Amplifier ii) Schmitt Trigger [NOV/DEC 2013], [NOV/DEC 2014], [APR/MAY 2015] (Understand)

26. Explain the working of i) Precision Full wave rectifier ii) Integrator
[NOV/DEC 2013], [NOV/DEC 2014] [APR/MAY 2019] (Understand)

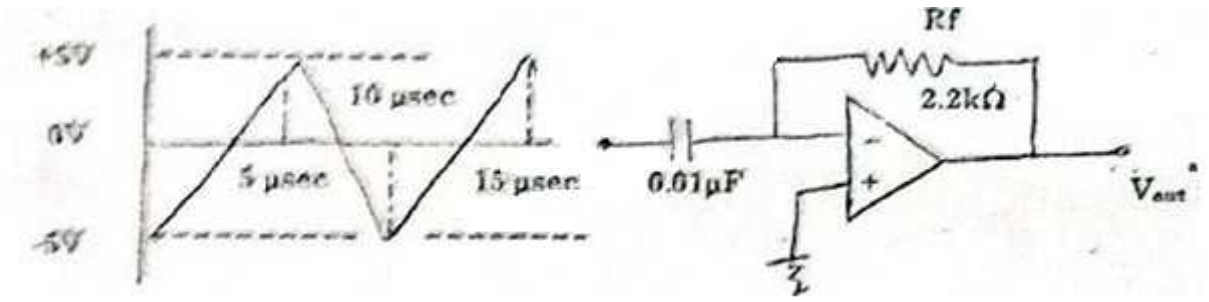
27. With the neat diagram explain logarithmic amplifier and Antilogarithmic Amplifier [MAY/JUNE 2014], [APR/MAY 2015] (Apply)

28. With neat diagram explain the application of op amp as precision rectifier, Clipper, and Clamper. (Understand) [MAY/JUNE 2014]

29. Explain in detail about V –I and I-V convertor. (Understand) [APR/MAY 2015]

30. Design a wide band pass filter with f_L= 400Hz, f_H= 2 kHz and a pass band gain of 4.Find the value Q of the filter. (Analyze) [APR/MAY 2015]

31. Determine the rate of change of the output voltage in response to the first input pulse as shown below for the integrator. The output voltage is initially zero. Also describe the output after the first pulse. Draw the output waveform.(8) (Apply) [APR/MAY 2015]



32. Explain in detail about the V to I and I to V converters. (Understand) (8) [APR/MAY 2015]

33. With a neat circuit diagram, explain the working of the precision rectifier. (8) (Understand) [Nov / Dec 2015]

34. Explain the application of operational amplifier as differentiator. (8) (Understand)[Nov / Dec 2015]

35. Mention two advantages of active filter over passive filter. Also design a second order low pass filter using operational amplifier for the upper cut off frequency of 2 kHz. Assume the value of capacitor to be 0.1μF. (8) (Apply) [Nov / Dec 2015]

36. With a neat circuit diagram explain the working of voltage to current converter.(8) (Apply) [Nov / Dec 2015] 37. Explain the working of an op-amp differentiator and derive its output equation. (8) (Apply) [R2008 Nov / Dec 2015]

38. What is the need for V to I and I to V converter? How are they realized using op-amp? (8) (Understand) [R2008 Nov / Dec 2015]

39. What is the purpose of a precision rectifier? How are they realized using op-amp? Explain (8) (Understand) [R2008 Nov / Dec 2015]

40. Draw the regenerator comparison circuit and obtain expression for UTP and LTP (8) (Apply) [R2008 Nov / Dec 2015]

41. Draw the circuit diagram of an instrumentation amplifier and explain its operation. List few applications. (12) [Apr/May 2018] [Nov / Dec 2018] [APR/MAY 2016] (Apply)

42. How an op-amp can be used as an Log amplifier (4) (Understand) [APR/MAY 2016]

43. Design a second order high pass Butterworth filter having cut off frequency of 5Khz. (6) (Analyze) [APR/MAY 2016]

44. What is a precision rectifier? With circuit schematic explain the working principle of full wave rectifier. (6) (Understand) [APR/MAY 2016]

45) Differentiate between low pass, high pass, band pass and band reject filter. Sketch the frequency plot. (Understand) (Nov /Dec 2016)

46) Design a second order low pass Butter worth filter for a cut off frequency of 1 KHz. (Nov /Dec 2016) Create

47) Write short notes on : Clipper and clamper circuits. And Integrater. (Nov /Dec 2016) (Remember)

48) With neat figures describe the circuit using Op Amps on the functioning of Integrator and double integrator circuit First order High pass filter. (April/May 2017) (Remember)

49) With neat figures describe the circuit using OpAmps on the operation of Zero cross Detecter, Clipper and damper circuits Scmitt Trigger. (April/May 2017) (Remember)

50) For performing differentiation in an operational amplifier, integtator is preferred to differentiator ? Explain.[Nov/Dec 2017](Analyze)

51) What is an instrumentation amplifier ? Draw a system whose gain is controlled by a variable resistance? .[Nov/Dec 2017] (Understand)

52) Design a clipper circuit for a clipping level of +0.61"V, given an input sinewave signal of 0.5V peak. Assume the gain of the amplifier is 12 and ithas an input resistance of 1k-ohm connected. [Nov/Dec 2017] (Understand)

53) Design a second ord.er Butterworth low-pass filter having upper cut-off frequency of 2.5 kHz. [Nov/Dec 2017] (Apply)

54) Design a differentiator to produce an output of 4Vwhen the input changes by 2V in 60 micro seconds. [Nov/Dec 2017] (Create)

55) i) Describe about voltage follower circuit.

ii) Write short notes on subtractor circuit.

56) Present the inverting and non inverting amplifier circuits of an opamp in closed loop configuration.Derive the expression for the closed loop gain these circuits. (Understand) [NOV/DEC 2018]

57) Design a second ord.er Butterworth low-pass filter having upper cut-off frequency of 2.1961 kHz. [Nov/Dec 2018] (Apply)

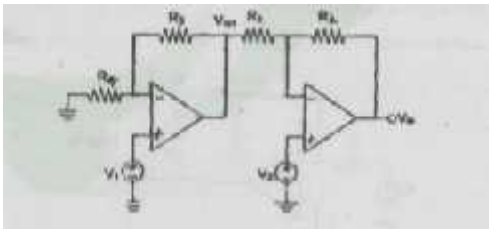
58) Design a clipper circuit for a clipping level of -0.83 V,given an input sine wave signal of 0.3Vpeak.Assume the gain of the amplifier is 9and it has an input resistance of 2.2 kOhm connected. [Nov/Dec 2018] (Apply)

59) Draw the operational diagram and explain the working principle of antilogarthmic amplifier and Schmitt trigger [Nov/Dec 2018] (Understand)

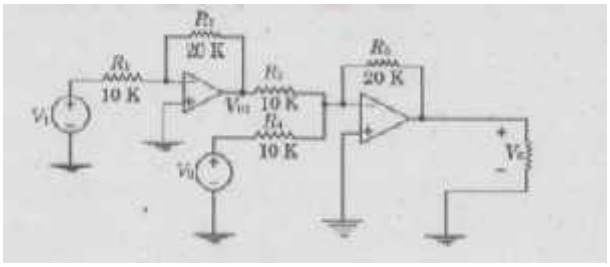
60) Design a differentiator to produce an output of 6Vwhen the input changes by 2V in 40 micro seconds. [Nov/Dec 2018] (Create)

61)Find Vo.Verify that if R3/R4 = R1/R2,the circuit is an instrumentation amplifier with gain A=1+R2/R1

[April/May 2019] (Remember)



62) Find the output expression for the figure shown. [APR/MAY 2019](Apply)



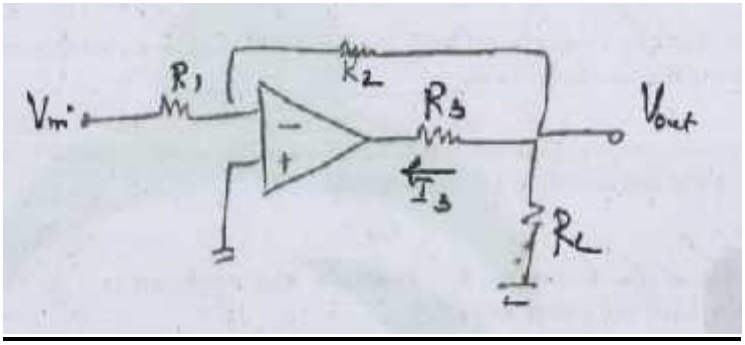
63) Explain the issues and challenges in active filter design with example. [APR/MAY 2019] (Understand)

64) The circuit given is inverting amplifier except the resistor R3 is added.The circuit parameters are R_1= 5KΩ, R_2=25kΩ, R_3 = 12.5 kΩ, R_l=5kΩ. [APR/MAY 2019](Analyze)

i)Derive Vout expression .

ii) Derive expression for I3.

iii)What happens to I3 if R3 is doubled? (R3= 25 kΩ)



ASSIGNMENT QUESTIONS

1. Using IC741,design a capacitor coupled non inverting amplifier circuit to operate with a 24v supply. The voltage gain is 100,output amplitude is 6V and lower cut –off frequency is to be 100 Hz to drive a minimum load resistance of 5.6kΩ. (PO3)(CREATE)

2. For the instrumentation amplifier using two ideal opamp shown in Fig.1 verify the equation (PO2)(UNDERSTAND)

$$Vo = (1 + R_2/R_1 + 2R_2/R_3)\,(V2-V1)$$

3. Prove that the voltage gain and input resistance with feedback of an inverting amplifier is given by

Avf = (- Arf) / (R1(1+A)+ Rf) and Rif = (R1+ Rf/(1+A)) ‖Ri (PO2)(ANALYZE)

4. Design an adder circuit using an opamp to get the output expression as Vo= - (0.1V1+V2+10V3). (PO3)(CREATE)

5. Design an opamp differentiator that will differentiate an input signal with Fmax=100 Hz. (PO3)(CREATE)

Draw the output waveform for a sinewave of 1V peak at 100 Hz applied to the differentiator.

6. Consider the lossy integrator.For component values R1=10K, Rf= 100K, Cf=10nF, Determine the lower limit of integration. (PO1)(REMEMBER)

7. Design a second order butterworth Low pass filter having upper cut off frequency 1 KHz. (PO3)(CREATE)

8. Find the output voltage vo of the given circuit when input Vi=10mV,Vi=100 mv and Vi=1V. (PO1)(REMEMBER)

9. Design a circuit to implement Vo =0.545V3+0.273V4- 1.25 V1- 2V2. (PO3)(CREATE)

10. Calculate Vo of the output current in given circuit if E1 equals i)+5V ii) – 2V.

For each situation, state if the opamp sources or sinks. (PO2)(ANALYZE)

UNIT – III

ANALOG MULTIPLIER AND PLL

Analog Multiplier using Emitter Coupled Transistor Pair - Gilbert Multiplier cell – Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing and clock synchronization.

PART - A

1. List the basic building blocks of PLL [Apr/May 2019] (Remember)

1. Phase detector/comparator
2. Low pass filter
3. Error amplifier
4. Voltage controlled oscillator

2. Define FSK modulation. (Remember) (MAY 2010)

FSK is a type of frequency modulation, in which the binary data or code is transmitted by means of a carrier frequency that is shifted between two fixed frequencies namely mark (logic1) and space frequency (logic 0).

3. What is analog multiplier? (Remember) (MAY 2010)

A multiplier produces an output v0, which is proportional to the product of two inputs vx and vy V0= kvxvy

4. List out the various methods available for performing for analog multiplier. (Remember)

- Logarithmic summing technique
- Pulse height /width modulation technique
- Variable Tran's conductance technique
- Multiplication using gilbert cell
- Multiplication technique using Trans conductance technique

5. Mention some areas where PLL is widely used. (Remember) (DEC 2009)

1. Radar synchronizations
2. Satellite communication systems
3. Air borne navigational systems
4. FM communication systems
5. Computers.

6. What are the three stages through which PLL operates? (Remember)

1. Free running
2. Capture
3. Locked/ tracking

7. Define lock-in range of a PLL. (Remember) [Nov/Dec 2017,MAY 2010] [Nov / Dec 2015]

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. It is expressed as a percentage of the VCO free running frequency.

8. Define capture range of PLL. (Remember) [Nov/Dec 2017,MAY 2010] [Nov / Dec 2015]

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. It is expressed as a percentage of the VCO free running frequency.

9. Define Pull-in time. (Remember) [R2008Nov / Dec 2015]

The total time taken by the PLL to establish lock is called pull-in time. It depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

10. Write the expression for FSK modulation. (Remember) (MAY 2010)

$\Delta vf=f2-f1/k0$

11. Define free running mode. (Remember) (MAY 2010)

An interactive computer mode that allows more than one user to have Simultaneous use of a program.

12. For perfect lock, what should be the phase relation between the incoming signal and VCO output signal? (Understand)

The VCO output should be 90 degrees out of phase with respect to the input signal.

13. Give the classification of phase detector: (Remember)

1. Analog phase detector.

2. Digital phase detector

14. What is a switch type phase detector? (Remember)

An electronic switch is opened and closed by signal coming from VCO and the input signal is chopped at a repetition rate determined by the VCO frequency. This type of phase detector is called a half wave detector since the phase information for only one half of the input signal is detected and averaged.

15. What is a voltage controlled oscillator? (Remember)

Voltage controlled oscillator is a free running multivibrator operating at a set frequency called the free running frequency. This frequency can be shifted to either side by applying a dc control voltage and the frequency deviation is proportional to the dc control voltage.

16. Define Voltage to Frequency conversion factor. (Remember)

Voltage to Frequency conversion factor is defined as,

$Kv = fo / Vc = 8fo / Vcc$

Vc is the modulation voltage

fo-frequency shift

17. What is the purpose of having a low pass filter in PLL? (Remember)

*It removes the high frequency components and noise.

*Controls the dynamic characteristics of the PLL such as capture range, lock-in range, band-width and transient response.

*The charge on the filter capacitor gives a short- time memory to the PLL

18. Discuss the effect of having large capture range. (Understand)

The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the frequency goes beyond the lock-in range. Thus, to increase the ability of lock range, large capture range is required. But, a large capture range will make the PLL more susceptible to noise and undesirable signal.

19.Mention some typical applications of PLL: (Remember) [APR/MAY 2015]

- Frequency multiplication/division
- Frequency translation
- AM detection
- FM demodulation
- FSK demodulation.

20. What is a compander IC? Give some examples. (Remember) (DEC 2009)

The term companding means compressing and expanding. In a communication system, the audio signal is compressed in the transmitter and expanded in the receiver. Examples: LM 2704-LM 2707; NE 570/571.

21. What are the merits of companding? (Remember)

*The compression process reduces the dynamic range of the signal before it is transmitted.

*Companding preserves the signal to noise ratio of the original signal and avoids non linear distortion of the signal when the input amplitude is large.

*It also reduces buzz, bias and low level audio tones caused by mild interference.

22. What is a VCO? (Remember) [APR/MAY 2010]

VCO is a free running multivibrator which operates at free running **frequency.**

23.Draw the relation between the capture ranges and lock range in a PLL. (Apply)

[APR/MAY 2010]

24. What is lock range and capture range of PLL? [NOV/DEC 2010] [NOV/DEC 2013] [Apr/May 2021] (Remember)

Range of frequencies over which PLL can maintain lock with the incoming signal is called lock range. Range of frequencies over which PLL can acquire lock with the incoming signal is called capture range.

25. With reference to a VCO, define voltage to frequency conversion factor *Kv*. (Remember)

[APR/MAY 2011]

$$Kv = \Delta fo / \Delta Vc$$

26. What are the advantages of variable transconductance technique? (Remember)

[APR/MAY 2012]

1. Provides four quadrant operation.
2. Good accuracy.
3. High speed operation.
4. Less error.

27.VCO is called v-f converter? why? (Understand) [**APR/MAY 2012]**

The frequency deviation is directly proportional to the dc control voltage and hence it is called a V-f converter.

28. A PLL frequency multiplier has an input frequency of "f" and a decade counter is included in the loop. What will be the frequency of the PLL output? [May / June 2013](Apply)

Output of PLL = 10f

29. Mention any two applications of PLL. (Remember) [May / June 2013] Frequency Translation & AM Detection.

30. What is meant by Frequency synthesizing. (Remember) [NOV/DEC 2013]

Large number of desired frequencies can be produced from a single crystal controlled oscillator

32. What is the need for Frequency Synthesizer. (Remember) [MAY/JUNE 2014]

To produce precise series of frequencies from a stable crystal oscillator

33. What is the function of phase detector in PLL? (Remember) [NOV/DEC 2014]

The phase detector produces a DC or low frequency signal which is proportional to the phase difference between the input signal and VCO output signal

34. Under what condition the gilbert cell will function as a multiplier? (Remember)

[**APR/MAY 2015]**

When both the input to the gilbert cell are very small, it will work as a multiplier.

35. How do you convert a basic multiplier to a squaring and square root circuit? (Understand)

[**APR/MAY 2015]**

When the input is connected to both the terminals of the multiplier IC, it will act as a squaring circuit

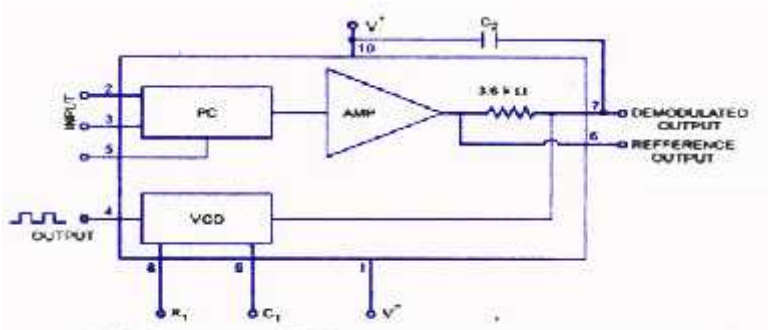
36. **Mention two application of analog multiplier**. **(Remember) [NOV/DEC 2015]**

Gilbert cell ,two and four quadrant multiplier**.**

37. With the equations, show how is a multiplier cab be used for finding phase angle difference between two signals. (Remember) [R2008 Nov / Dec 2015]

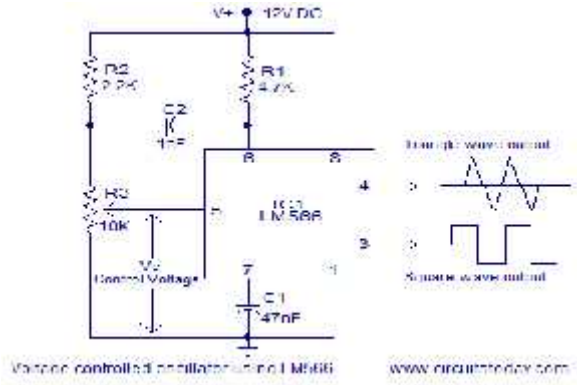
38. What is four quadrant multiplier? (Remember) [APR/MAY 2016]

39. Draw the circuit diagram of PLL circuit using as a FM detector. [APR/MAY 2016]



Block Diagram of PLL Unit 566 For Use As FM Detector

40) Draw the block diagram of IC 566 VCO (Voltage Controlled Oscillator). (Nov/Dec 2016) Remember



41) Enlist any four applications of NE 565 PLL. [Nov/Dec 2016] [Nov/Dec 2018] Remember

Frequency Multiplier

Frequency Translator (frequency Synthesizer)

FM Detector

FSK Demodulator

42) **How is frequency stability obtained in a PLL by use of a VCO? (April/May 2017) (Remember)**

Harmonic oscillator VCOs have these advantages over relaxation oscillators:

- Frequency stability with respect to temperature, noise, and power supply is much better for harmonic oscillator VCOs.
- They have good accuracy for frequency control since the frequency is controlled by a crystal or tank circuit

A disadvantage of harmonic oscillator VCOs is that they cannot be easily implemented in monolithic ICs

There are two reasons for using a Voltage-controlled crystal oscillators

- To adjust the output frequency to match or perhaps be some exact multiple of an accurate external reference.
- Where the oscillator drives equipment that may generate radio-frequency interference, adding a varying voltage to its control input can disperse the interference spectrum to make it less objectionable

43) Mention the need of pre-distortion circuits in Gilbert analog multiplier and how is the configuration of Gilbert multiplier done with pre-distortion circuits. [Nov/Dec 2017] (Remember)

44) State any two terminologies associated with multiplier characteristics.[Apr/May 2018](Remember)

Accuracy,Linearity,Bandwidth,scale factor,zero trim.

46)What is Gilbert multiplier cell? .[Apr/May 2018] [Nov/Dec 2018] [Apr/May 2019] (Remember)

A circuit which uses emitter coupled pair in series with a cross coupled emitter coupled pairs is called a Gilbert cell.This allows four quadrant operation.

47) List the features of VCO. [Apr/May 2021](Remember)

PART - B

1. Draw and explain the block diagram of PLL IC 565. (Understand) [NOV/DEC 2013]
2. Draw and explain the operation of VCO IC 566 and derive the expression for f_o. (Understand) [Nov'05]

3. a) Derive the expression for capture range and lock range of PLL. (10)(Apply)
   b) Derive the expression for voltage to frequency conversion factor of VCO. (6) (Apply) [Nov'07]
4. Explain the application AM detector and FSK demodulator using PLL. (Understand)
5. Explain various types of phase detectors used in PLL. (Understand)
6. a) Explain the application frequency synthesizer using PLL.(8) (Understand) (Nov/Dec 2016)
   b) What is the function of LPF in PLL? (8) (Remember) [Nov'05]
7. Draw and explain the block diagram of PLL IC 565 and derive its transfer function. (Understand)
8. Draw and explain the operation of VCO IC 566 and derive the expression for f_o. (Understand) [Nov'05]

9. a) Derive the expression for capture range and lock range of PLL. (10) (Apply) [APR/MAY 2019] [APR/MAY 2015][Nov'07]
   b) Derive the expression for voltage to frequency conversion factor of VCO. (6)
10. Explain about Analog multiplier IC. (Understand) [APR/MAY 2018][APR/MAY 2015]

11. Sketch and explain the following applications of multipliers. [Apr '11]
    1. Squaring (4)
    2. Finding square root (4)
    3. Frequency doubler (4)
    4. Phase angle detector (4) (Understand)

12. (i) With a neat diagram explain the variable transconductance technique in analog multiplier and give its output equation. (8) (Apply) (Nov/ Dec 2016)

(ii) Briefly explain the working of voltage controlled oscillator. (8) (Understand) [APR/MAY 2010] [NOV/DEC 2018]

13. What are important building block of phase locked loop (PLL) explain its Working? (Understand) [APR/MAY2010] [APR/MAY 2015]

14. Draw the functional block schematic of a NE565 PLL and explain the roles of the low pass filter and VCO. Derive the expression for the capture range and lock in range of the PLL. (Understand)) (Nov/ Dec 2016) [NOV/DEC 2010]

15. With suitable block diagram, explain the operation of 566 voltage controlled oscillator. Also derive an expression for the frequency of the output waveform generated.(Apply) [NOV/DEC 2010]

16.(i)List and define the various performance parameters of a multiplier IC. (Remember) [MAY/JUN 2012]

(ii) How the multiplier is used as the voltage divider? (Understand)

(iii) How the multiplier is used as the frequency doubler? (Understand)

17. (i) Explain with neat block diagrams how PLL is used as [APR/MAY 2019]

(i) AM detector [NOV/DEC 2014]

(ii) FM detector [NOV/DEC 2013][NOV/DEC 2014] [NOV/DEC 2018]

(iii) Frequency synthesizer (iv) FSK Demodulation [NOV/DEC 2018] (Understand) [MAY/JUN 2012] , [MAY/JUNE 2014]

18. a) i) What do you mean by variable Trans conductance Analog multiplier? (Remember)

ii) State the advantages of variable Transconductance technique for analog multiplication. (Remember)

iii) Draw the circuit and explain the working of one quadrant variable Trans conductance analog multiplier. (Understand) [May / June 2013]

19. Draw the block diagram and explain principle of working, characteristics and applications of

i) Frequency synthesizer.

ii) Frequency shift keying (FSK) Demodulator. (Understand) [May / June 2013]

20. Explain the working of Gilbert Multiplier cell (Understand) [NOV/DEC 2013] **.[APR/MAY2021]**

21. Explain the principle of operation of PLL?(Understand) [APR/MAY 2018][NOV/DEC 2013] [NOV/DEC 2018]

22. Explain the working of Analog Multiplier using emitter coupled transistor pair. Discuss the application of analog multiplier IC. (Understand) [MAY/JUNE 2014] [NOV/DEC 2014] [NOV/DEC 2018]

23. Explain the application of VCO for FM generation. (6) (Understand) [APR/MAY 2015]

24. With neat simplified internal diagram, explain the working principle of Operational Tran's conductance amplifier. (OTA).(10) (Understand) [APR/MAY 2015]

25. Define capture range and lock range. Explain the process of capturing the lock and also drive for capture range and lock range. (16) (Apply) [APR/MAY 2015]

25. Derive the expression for the capture range and lock range of Phase Locked (16) [NOV/DEC 2015] (Apply)

26. Explain the application of PLL as (16) [NOV/DEC 2015]

(i).Frequency synthesizer

(ii)AM demodulator and

(iii) FM demodulator (Understand)

27. Explain the working of Analog Multiplier using emitter coupled transistor with circuit diagram. (8) (Understand) [R2008NOV/DEC 2015]

28. Describe how a PLL could be used as a voltage controlled oscillator. (8) (Analyze)

[R2008 NOV/DEC 2015]

29. Draw the basic schematic of the PLL and explain its operation. (8) (Understand)

[R2008 NOV/DEC 2015]

30. Explain the functional diagram the FSK modulation and demodulation operations using PLL's (8) (Understand) [R2008 NOV/DEC 2015] **.[APR/MAY2021]**

31. Explain the working principle of four quadrant variable form trasconductance multiplier. (Understand) [APR/MAY 2016]

32. Discuss the principle of operation of NE565 PLL circuit. (10) (Understand) [APR/MAY 2016]

33. How can PLL be modeled as a frequency multiplier? (6)(Understand) [APR/MAY 2016]

34) With neat diagram explain the design of (i) Frequency Synthesizer
(ii) Frequency Division circuit using PLL IC 565. (APR/MAY 2017) (Remember)

35) With neat figures explain the emitter couple circuit based design of(i) Gilbert multiplier cell for four quadrant. multiplication (ii) the operation of VCO. (APR/MAY 2017) (Remember)

36) With a neat figures design a PLL with free running frequency of 500 kHz and the bandwidth of low pass filter is 50 kHz. Will the loop acquire lock for an input signal of 600 kHz. Justify your answer. Assume that phase detector needs to produce sum and difference frequency components. (APR/MAY 2017)

37) Write notes on basic analog multiplication techniques. [Nov/Dec 2017](Remember)

38) Explain the operation of a variable transconductance multiplier circuit.Derive the expression for its output voltage. [Nov/Dec 2017](Understand)

39) Derive the expression for free running frequency of voltage controlled oscillator? [Nov/Dec 2017](Understand)

40) Explain the process of FSK demodulation using PLL. How is the stability of the frequency obtained in a PLL by the use of voltage controlled oscillator. [Nov/Dec 2017] (Understand)

41) A PLL has a free running frequency of 400 kHz and the band-width of the low pass filter is 8 kHz. Will the loop tend to acquire lock for an input signal of 550 kHz? Explain. In this case, assume that the phase detector produces sum and difference frequency components. [Nov/Dec 2017] (Analyze)

42) Explain in detail about VCO using suitable diagram[Apr/May 2018](understand)

43) A PLL has a free running frequency of 600 kHz and the band-width of the low pass filter is 4 kHz. Will the loop tend to acquire lock for an input signal of 520 kHz? Explain. In this case, assume that the phase detector produces sum and difference frequency components. [Nov/Dec 2018] (Analyze)

ASSIGNMENT QUESTIONS

1. Design a VCO having the maximum range of 1KHz.Assume power supply Vcc=15V.Required pulse width should not exceed 100µs. (PO3)(CREATE)
2. Design PLL 565 as a FSK demodulator in telephone data transmission. (PO3)(CREATE)
3. Design a PLL circuit using IC565 to get free running frequency of 4.5 KHz.,Lock range of 2 KHz, Capture Range of 100Hz.Assume supply voltages of ±10Vare available.Show diagram with all component values. (PO3)(CREATE)
4. In basic multiplier circuit,calculate the output voltage Vo with input voltages Vi=4V and reference voltage Vref=10V. (PO1)(REMEMBER)
5. For a VCO circuit,assume R2=2.2KΩ ,R1=R3 = 15K and C1= 0.001µF.Assume Vcc=12V. Determine i) output frequency ii)the change in output frequency if modulating input Vc is varied from 7 to 8V. (PO2)(ANALYZE)
6. Determine the change in dc control voltage Vc during lock, if input signal frequency fs=20KHz,the free running frequency is 21KHz and voltage to frequency transfer coefficient of VCO is 4 KHz/V. (PO1)(REMEMBER)
7. A PLL IC565 connected as an FM demodulator has R1=10KΩ, C1= 0.01µF and C2= 0.04µF.The supply voltage is +12 V. Determine the i) Free running frequency ii) Lock in range iii) Capture range. (PO1)(REMEMBER)
8. In the given circuit V+= 12V,R2= 1.5K,R1=R3=10K and C1= 0.001µF. i) Determine nominal frequency of output. Ii) Compute modulation in output frequencies if Vc is varied between 9.5 and 11.5V. iii) Draw square wave output waveform if the modulating input is a sinewave. (PO2)(UNDERSTAND)

UNIT – IV

ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

Analog and Digital Data Conversions, D/A converter – specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R - 2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type – Dual Slope type - A/D Converter using Voltage-to-Time Conversion - Over-sampling A/D Converters, Sigma – Delta converters.

PART - A

1. Name the essential parts of a DAC. (Remember) (MAY 2010)

- Drive motors
- Analog devices
- Deglitcher
- Filter

2. Write down the drawback of weighted D/A converter. (Remember)

The main disadvantage of binary weighted D/A converter is the requirement of wide range of resister values. As the length of the binary word is increased .the range of resister values needed also increases.

3. List the broad classification of ADCs. (Remember)

1. Direct type ADC**.**
2. Integrating type ADC.

4. List out the direct type ADCs. (Remember) (DEC 2009)

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter
4. Successive approximation type converter

5. List out some integrating type converters. (Remember)

1. Charge balancing ADC
2. Dual slope ADC

6. What is integrating type converter? [Apr/May 2021](Remember)

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter.

7 .Explain in brief the principle of operation of successive Approximation ADC. (Remember)

The circuit of successive approximation ADC consists of a successive approximation register (SAR), to find the required value of each bit by trial & error. With the arrival of START command, SAR sets the MSB bit to 1. The O/P is converted into an analog signal & it is compared with I/P signal. This O/P is low or High. This process continues until all bits are checked.

8. What are the main advantages of integrating type ADCs? (Remember)

a. The integrating type of ADC's do not need a sample/Hold circuit at the input.

b. It is possible to transmit frequency even in noisy environment or in an isolated form.

9. Where are the successive approximation type ADC's used? (Remember)

The Successive approximation ADCs are used in applications such as data loggers & instrumentation where conversion speed is important.

10. What is the main drawback of a dual-slop ADC? (Remember) (DEC 2009)

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC

11. State the advantages of dual slope ADC. (Remember) (DEC 2009)

It provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T.

12. Define conversion time. (Remember) (DEC 2009)

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used & the propagation delay of circuit components. The conversion time of a successive approximation type ADC is given by T(n+1) where T---clock period Tc---conversion time n-- -- no. of bits

13. Where are the successive approximation type ADC's used? (Remember)

The Successive approximation ADCs are used in applications such as data loggers & instrumentation where conversion speed is important.

14. What is the main drawback of a dual-slop ADC? (Remember)
(DEC 2009)

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC

15. State the advantages of dual slope ADC (Understand) (DEC 2009)

It provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T.

16. Define conversion time. (Remember) (DEC 2009)

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used & the propagation delay of circuit components. The conversion time of a successive approximation type ADC is given by T(n+1)

where T---clock period

Tc---conversion time

n----no.of bits

17. Define resolution of a data converter. (Remember) (MAY 2010)

The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter. Resolution (in volts)= VFS/2n-1=1 LSB increment. The resolution of an ADC is defined as the smallest change in analog input for a one bit change at the output.

18. Define accuracy of converter. (Remember) (MAY 2010)

Absolute accuracy:

It is the maximum deviation between the actual converter output & the ideal converter output.

Relative accuracy:

It is the maximum deviation after gain & offset errors have been removed. The accuracy of a converter is also specified in form of LSB increments or % of full scale voltage.

19. What is settling time? [Apr/May 2019] (Remember)

It represents the time it takes for the output to settle within a specified band ±½LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitance & inductances. Settling time ranges from 100ns. 10Ws depending on word length & type circuit used.

20. Explain in brief stability of a converter: (Understand)

The performance of converter changes with temperature age & power supply variation. So all the relevant parameters such as offset, gain, linearity error & monotonicity must be specified over the full temperature & power supply ranges to have better stability performances.

21. What is meant by linearity? (Remember)

The linearity of an ADC/DAC is an important measure of its accuracy & tells us how close the converter output is to its ideal transfer characteristics. The linearity error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ±½LSB.

22. What is monotonic DAC? (Remember)

A monotonic DAC is one whose analog output increases for an increase in digital input.

23. What are the specifications of D/A converter? (Remember)

The specifications are accuracy, offset voltage, monotonicity, resolution, and settling time.

24. What is a sample and hold circuit? Where it is used? [MAY/JUNE2014], [NOV/DEC 2014] [NOV/DEC 2018] (Remember)

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

25 .Define sample period and hold period. (Remember) (DEC 2009)

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period. The time period during which the voltage across the capacitor is held constant is called hold period.

26. Which is the fastest ADC and why? (Remember) (MAY 2010)

Simultaneous type A/D converter (flash type A/D converter) is the fastest because A/D conversion is performed simultaneously through a set of comparators.

27. What are the advantages and disadvantages of R-2R ladder DAC? (MAY2010) [Apr/May 2021] (Remember)

Advantage:

• Easier to build

• Number of bits can be expanded by adding more sections.

Disadvantage:

• More power dissipation makes heating, which in turns develops non-linearties in DAC.

28. Give the disadvantages of flash type A/D converter. (Remember) (MAY 2010)

The simultaneous type A/D converter is not suitable for A/D conversion with more than 3 or 4 digital output bits. Then (2n- 1) comparators are required for an n-bit A/D converter and the number of comparators required doubles for each added bit.

29. Define quantization error. (Remember)

In A/D converter the smallest digital step is due to the LSB and it can be made smaller only by increasing the number of bits in the digital representation. This error is called quantization error.

30. Define Dither. (Remember)

It is a very small amount of random noise (white noise) which is added to the input before A/D conversion to improve the performance of A/D converter.

31. Define Delta modulation. (Remember)

Delta modulation is a technique in which derivative of the signal is Quantized. The delta modulation shows slope overload for fast input signals and their performance is dependent on input signal frequency.

32. Define slope overload noise and granular noise. (Remember)

Slope overload noise is introduced due to the use of a step size delta is too small to follow some portions of the waveform with a step size. Granular noise results from using a step size that is too large in parts of the Waveform having a small slope.

33. Define resolution of a data converter.[APR/MAY 2010] , [NOV/DEC 2010]& [APR/MAY2011], [NOV/DEC 2014] (Remember)

Resolution of a converter is a smallest change in voltage which may be produced at the output.

34. Give the advantages of integrating type ADC. (Remember) [APR/MAY 2010]

Integrating type ADC perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to digital code. Here accuracy is more.

35. Compare and contrast binary ladder and R-2R ladder DAC? (Analyze) [NOV/DEC 2010]

Binary ladder DAC:

Requires wide range of resistor values.

R-2R ladder DAC:

Only two resistor values are required.

36. Define conversion time of DAC. (Remember) [NOV/DEC 2010], [APR/MAY2011]

It is the total time required to convert digital signal into analog signal.

37. Define following performance parameters of D/A converters: (Remember) [APR/MAY2011]

Accuracy:

It is the maximum deviation between the actual converter output and the ideal converter output.

Monotonicity: **[APR/MAY2015]**

Monotonic DAC is the one whose analog output increases for an increase in digital input.

38. Which is the fastest ADC? State the reason. (Understand) [APR/MAY 2011]

Flash type ADC is the fastest ADC as the conversion takes place simultaneously rather than sequentially.

39. Define settling time of D/A converter. (Remember) [APR/MAY 2012]

Time taken for the output to settle within specified band $\pm$ ½ LSB of its final value.

40. What is the main drawback of dual slope ADC (Remember) [APR/MAY 2012] Long conversion time

41. Mention any two specifications of a D/A converter. (Remember)[May / June 2013]

Accuracy & Resolution.

42. For an n-bit flash type A/D converter, how many comparators are required? State the disadvantage of that type of converter.[May / June 2013] (Understand)

$2^n - 1$.

43. State the principle of single slope A/D Converter (Understand) [NOV/DEC 2013]

It uses a integrator to generate a sawtoothwafeform which is then compared against the analog input by a comparator

44. Give any two advantages of SA type ADC (Remember) [MAY/JUNE 2014]

Efficient

Conversion speed is more

45. What is over sampling? (Remember) [APR/MAY 2015]

Oversampling converters sample the analog signal at a rate much higher than the sampling rates normally required with nyquist converters.

46. What would be produced by a DAC whose output range is 0-10v and whose input binary number is 10111100 (for a 8 bit DAC)? (Apply) [APR/MAY 2015]

$V_0 = 10V\ [1/2^1+0/2^2+1/2^3+1/2^4+1/2^5+1/2^6+0/2^7+0/2^8]$

$= 10[47/64]$

$= 7.34$ V

47. Determine the number of comparators and resistors required for 8 bit flash type ADC. (Apply) [NOV/DEC 2015]

48. Mention two advantages of R-2R ladder type Digital to Analog converter when compared to weighted resistor type Digital to Analog Converter. (Remember) [NOV/DEC 2015]

49. Why is an interval R-2R ladder network DAC better than R-2R ladder DAC? (Remember) [R2008 NOV/DEC 2015]

50. Which is the fastest ADC and Why? (Remember) [R2008 NOV/DEC 2015]

51. A 12 bit D/A converter has resolution of 20mV/LSB. Find the full scale output voltage. (Apply) [APR/MAY 2016]

52. Draw the binary ladder network of DAC. If the value of the smaller resistance is 10k, what is the value of the other resistance? (Apply) [APR/MAY 2016]

53) What are the advantages of inverted R – 2R (current type) ladder D/A

converter over R– 2R (voltage type) D/A converter? (Nov/Dec 2016) (Remember)

Advantages:
• It is Simple in Construction.
• It provides fast conversion.

Disadvantages:
• This type requires large range of resistors with necessary high precision for low resistors.
• Requires low switch resistances in transistors.
• Can be expensive. Hence resolution is limited to 8-bit size.

Advantages:
• Only two resistor values are used in R-2R ladder type.
• It does not need as precision resistors as Binary weighted DACs.
• It is cheap and easy to manufacture.

Disadvantages:
• It has slower conversion rate.

For N bit DAC:
• Number of different levels = 2^N
• Number of Steps = $2^N - 1$

Resolution or step size of DAC = Analog output/Number of steps = $Va/(2^N - 1)$

% Resolution = (Step Size/Full scale output) x 100 %

54) What is the need for electronic switches in D/A converter? (Nov/Dec 2016) (Understand)

Although switches can be made of using diodes, Bipolar junction Transistors,
Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are
i) Switches using overdriven Emitter Followers.
ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

iii) CMOS switch for Multiplying type DACs .
iv) CMOS Transmission gate switches.
These configurations are used to ensure the high speed switching operations for different types of DACs.

55) Why are Scottky diodes used in sample- and- hold circuits?
A forward-biased Schottky diode does not have any minority carrier charge storage. This allows them to switch more quickly than regular diodes, resulting in lower transition time from the sample to the hold step.

56) How is the classification of A/D converters carried out based on their operational features ? [Nov/Dec 2017](Remember)
Single slope ADC
Dual slope ADC
Successive Approximation ADC
Flash ADC

57) Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values. [Nov/Dec 2017](Remember)

Eight resistors are required for an 8-bit weighted resistor D/A converter.2^0R , 2^1R, 2^2R, 2^3R, 2^4R, 2^5R, 2^6 R, 2^7R.

58) Define Sampling. [APR/MAY 2018](Remember)

Sampling is the reduction of a continuous-time signal to a discrete-time signal.

59)Differentiate between direct type and integrating type ADC convertors. [Nov/Dec 2018](Remember)

Direct type ADC compares a given analog signal with the internally generated equivalent signal. Integrating type ADC's perform conversion in an indirect manner by first changing the analog input signal to a function of time or frequency and then to corresponding digital code.

60)What is the largest value of output voltage from an 8 bit DAC that produces 1.0 V for a digital input of 00110010? [Apr/May 2019] (Remember)

PART - B

1. Draw and explain the functional diagram of the successive approximation ADC converter. (Understand) [Nov'06]

2. Explain the operation of R-2R ladder type DAC and the weighted resistor type DAC. (Understand) [Nov'05][Apr '11]

3. a) Draw and explain the operation of sample and hold circuits. (Understand) (8)

b) Explain the operation of voltage to time converter. (Understand) (8)

4. Explain the principle of operations. (16 [MAY/JUNE 2014][Nov'03]

a) Single slope ADC converter. [APR/MAY 2018]

b) Dual slope ADC converter. (Understand)

5. Explain the working of flash ADC. (Understand)

(Nov Dec 2016) [NOV/DEC 2014][MAY/JUNE2014][APR/MAY 2015]

6. An 8 bit DAC produces an output voltage '0v' corresponds to an input sequence'00000000'.if the DAC is connected for a basic increment of 10mv.

What is the output when input is '11111111'? (Apply) [EEE May'08]

7. a) A dual slope ADC uses a 16 bit counter and a 4 MHz clock rate. The

Maximum input voltage is =10V. The maximum integrator output voltage should be -8V when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1μF. Find the value of the resistor R of the integrator. If the analog signal is = 4. 129 V, find the corresponding binary number. (Apply) (8)

8. How many bits are required to design a DAC that can have a resolution of 5mV? The ladder has =8V full scale. (Analyze) (8)

9. Explain delta sigma modulation with required diagram. (Understand) (16)

10. What are the limitations in weighted resistor type D/A converters and explain how this problem can solve in R-2R ladder type D/A converters. (Understand) [NOV/DEC 2013][Apr '11]

11. (i) Explain the working of R-2R ladder DAC. (8) [APR/MAY 2019] [NOV/DEC 2018] (Understand)

(ii) Explain the working of successive approximation ADC. (8) (Understand) [NOV/DEC 2018] [APR/MAY 2010]

12. (i) A dual slope ABC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8V when the counter has recycled through n 2 counts. The capacitor used in the integrator is0.1μF. Find the value of resistor R of the integrator. (Apply) (8)

(ii) What is a sample and hold circuit? Briefly explain its construction and application. [APR/MAY 2010] (Understand)

13. Describe the operation of dual slope and successive approximation type ADC. What are the advantages of dual slope ADC? (Understand) [NOV/DEC 2013][NOV/DEC 2010], [APR/MAY 2015]

14.(i) Explain voltage mode and current mode operations of R-2R ladder type DAC.(Understand) [APR/MAY 2015]

(ii) Discuss the operation of sample and hold circuit with circuit diagram. [NOV/DEC 2010] (Understand) [APR/MAY 2015]

15.(i) Explain the following type of electronic switches used in D/A converter with suitable diagrams (1) Totem pole MOSFET switch (2) CMOS inverter as switch (Understand) [NOV/DEC 2018] [MAY/JUN 2012]

(ii) Explain the working of R-2R ladder DAC, by taking example of a 3 bit DAC circuit. Sketch the corresponding equivalent circuits and hence obtain the equation for output .(Apply)[NOV/DEC 2013]

16.(i)With neat circuit diagram and wave form of output, explain the working of dual slope A/D converter. (Understand) [NOV/DEC 2013][MAY/JUN 2012] **.[APR/MAY2021]**

(ii) Give a table of comparison of Flash, Dual slope and successive approximation ADC's in terms of parameters like Speed, Accuracy, resolution and input hold time.(Analyze)

17. (i) Compare single slope ADC and dual slope ADC. (Analyze)

(ii) Draw the circuit and explain the working of dual slope A/D converter. (Apply)

(iii) For a particular dual slope ADC, t1 is 83.33 ms and the reference voltage is 100mV. Calculate to if

1) V1 is 100 mv and
2) 200 mv. (Apply)

18. Draw the block diagram and explain the working of:

i) Charge Balancing VFCS

ii)Voltage to Time converter. (Understand) [May / June 2013]

19. Explain the weighted resistor type and R-2R type DAC. (Understand) [NOV/DEC 2014][MAY/JUNE 2014] [APR/MAY 2015]

20. What are oversampling data convertors? (Remember) [NOV/DEC 2018] [APR/MAY 2015]

21. With a neat block diagram, explain the working of Successive Approximation type Analog to Digital Converter. Also determine the conversion time of 8bit and 16 bit Successive Approximation type Analog to digital Converter if its clock frequency is 50Hz. [NOV/DEC 2015] (Apply)

22. With a neat block diagram, explain the working of two bit flash type analog to digital Converter. (Understand) [NOV/DEC 2015]

23. Design a suitable D/A converter to convert 8-bit binary input in parallel form. Binary '0'corresponds to 0V and binary '1' to 5V.Maximum output is +5V.Assume any other data that may be required. Explain its operation. (10) (Understand) [NOV/DEC 2015]

24. Write a note on high speed sample and hold circuits (6) (Understand) [NOV/DEC 2015]

25. With circuit diagram explain the operation of a flash type A/D Converter. (8) (Understand) [NOV/DEC 2015] [NOV/DEC 2018]

26. Compare the properties of Successive Approximation type and dual slope type converter (8) (Analyze) [NOV/DEC 2015]

27. Explain the successive approximation type A/D converter. (12) (Understand) [APR/MAY 2016]

28. Narrate the function of analog switches. (4) (Remember) [APR/MAY 2016]

29. State the significance of using high speed sample and hold circuits. Explain its working principle. (12) (Understand) [APR/MAY 2016]

30. Compare the performance of various DACS. (4)(Analyze) [APR/MAY 2016]

31) An 8 bit A to D converter accepts an input voltage signal of range 0 to 10 v.

What is the minimum value of the input voltage required to generate a change of 1 LSB?

What input voltage will generate all Ts at A to D converter output? (Nov/Dec 2016) (Understand)

32) With functional block diagram explain A/ D converter using voltage to time converter with input and output waveforms. (Nov/Dec 2016) (Understand)

33) How are A/D converters categorized?

(ii) Discuss on the successive approximation type ADC. (April/May 2017) (Remember)

34) What is meant by resolution, offset error in ADC,

(ii) Discuss on the dual slope type ADC. (April/May 2017) (Remember)

35) With a neat block diagram explain the stages for developing the signal analysis circuits required for an instrumentation module of say a vibration sensor data using instrumentation amplifier, wave shaper, comparator and ADC using OPAMP and required components. (April/May 2017) (Understand)

36) Explain in detail on the operational features of 4-bit weighted resistor type D/A converter.

[Nov/Dec 2017] (Understand) **.[APR/MAY2021]**

37) Differentiate between current mode and voltage mode R-2R ladder D/A converters.

[Nov/Dec 2017] (Understand)

38) With a neatblock diagram, explain the operation of successive approximation type A/D converter in detail. [Nov/Dec 2017] (Understand)

39) An 8-bit A/D converter accepts an input voltage signal of range 0 to 9V.What is the minimum value of the input voltage required for generating a change of 1 least significant bit ? Specify the digital output for an input voltage of 4 V. What input voltage will generate all ls at the A/D converter output ? [Nov/Dec 2017] (Apply)

40) For a 4-bit R-2R ladder D/A converter assume that the full scale voltage is 12 V. Calculate the step change in output voltage on input varying from 1001 to 1111. [Nov/Dec 2017] (Apply)

41)Enumerate the specifications of D/A converter [APR/MAY 2018](Understand)

42) For a 4-bit R-2R ladder D/A converter assume that the full scale voltage is 16 V. Calculate the step change in output voltage on input varying from 0111 to 1111. [Nov/Dec 2018] (Apply)

43)(i)Assume the following values for the ADC clock frequency = 1MHz; DAC has F.S. output =10.23V and a 10 bit input.Determine the following values. [APR/MAY 2019](Understand)

i) The digital equivalent obtained for the input voltage Va=3.728V.

ii)The conversion time.

iii)The resolution of this converter in percentage.

(ii) A 10 bit DAC has a step size of 10 mV.Determine the full scale output voltage and the percentage resolution.

ASSIGNMENT QUESTIONS

1. The basic step of a 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output is produced if the input is 101101111? (PO1)(REMEMBER)

2. Calculate the values of LSB, MSB and full scale output for an 8 bit DAC for 0-10 V range. (PO1)(REMEMBER)

3. What output voltage would be produced by a D/A converter whose output range is (0-10)V and whose binary input is i) 10(for 2 bit DAC) ii) 0110(4 bit DAC) iii) 10111100 (8 bit DAC). (PO1)(REMEMBER)

4. A Dual slope ADC uses a 16 bit counter and a 4MHz clock rate. The maximum input voltage is 10 V. The maximum integrator output voltage should be -8V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1µF.Find value of resister R of the integrator. Also find equivalent digital number for analog signal Va= 4.129V. (PO1)

(REMEMBER)

5. Compare the resolutions of 3 ½ DVM(digital voltmeter) and 4 ½ DVM which are commonly used in Laboratory. (PO2)(UNDERSTAND)

6. Consider R-2R 4 bit converter and assume feedback resistance Rf of opamp is variable, the resistance R=10K and Vr=10V.Determine the value of Rf that should be connected to achieve the following output condition. (PO1)(REMEMBER)

i). The value of 1 LSB at the output is 0.5 V
ii). The analog output of 6V for a binary input of 1000.
iii). The full scale output voltage of 12 v.
iv). The actual maximum output voltage of 10V.

7. A R-2R ladder network has 10 V reference voltage.The DAC produces a short circuit current of 1.875mA when a digital code 1111 is applied.Design a DAC for the above condition and Check the magnitude of short circuit current for an input code 1100. (PO3)(CREATE)

8. Find step size and analog output for 4 bit R-2R ladder DAC when input is 0111 and 1111.Assume Vref = +5V. (PO1)(REMEMBER)

9. A 10 bit A/D converter has an input voltage of -10V to +10 V. What is the resolution and percentage resolution. (PO1)(REMEMBER)

10. An A/D converter has a conversion time of 1µs.Calculate the maximum frequency at which it can be used. (PO1)(REMEMBER)

UNIT - V

WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator, Low Drop – Out(LDO) Regulators - Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Optocouplers and fibre optic IC.

PART - A

1. Mention some applications of 555 timer (DEC 2009) (Remember)

*Oscillator
*pulse generator
*ramp and square wave generator
*mono-shot multivibrator
*burglar alarm
*traffic light control.

2 . List the applications of 555 timer in monostable mode of operation: [NOV/DEC '13] (Remember)

*Missing pulse detector
*Linear ramp generator
*Frequency divider
*Pulse width modulation.

3. List the applications of 555 timer in Astable mode of operation: (Remember) (MAY/JUNE2010)[NOV/DEC 2013]

*FSK generator
*Pulse-position modulator

4. What is a voltage regulator? (Remember) (MAY 2010)

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

5. Give the classification of voltage regulators: (Remember) (MAY 2010)

*Series / Linear regulators

*Switching regulators.

6. What is a linear voltage regulator? (Remember)

Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region .The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.

7. What is a switching regulator? (Remember)

Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continously.This give improved efficiency over series regulators.

8. What are the advantages of IC voltage regulators? (Remember) (April /May 2017)

*low cost

*high reliability

*reduction in size

*excellent performance

9. Give some examples of monolithic IC voltage regulators: (Remember)

78XX series fixed output, positive voltage regulators

79XX series fixed output, negative voltage regulators

723 general purpose regulators.

10. What is the purpose of having input and output capacitors in three terminal IC regulators? [Apr/May 2021] (Remember)

A capacitor connected between the input terminal and ground cancels the Inductive effects due to long distribution leads. The output capacitor improves the transient response.

11. Define line regulation. (Remember) [NOV/DEC 2013], [NOV/DEC 2014] [APR/MAY 2018]

Line regulation is defined as the percentage change in the output voltage for a change in the input voltage. It is expressed in mill volts or as a percentage of the output voltage.

12. Define load regulation. (Remember) [NOV/DEC 2014]

Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.

13.What is meant by current limiting? (Remember) [APR/MAY 2015]

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

14. Give the drawbacks of linear regulators: **(Remember)**

*The input step down transformer is bulky and expensive because of low line frequency.

*Because of low line frequency, large values of filter capacitors are required to decrease the ripple.

*Efficiency is reduced due to the continuous power dissipation by the transistor as it operates in the linear region

15.What is the advantage of monolithic switching regulators? (Remember) (MAY 2010)

*Greater efficiency is achieved as the power transistor is made to operate as low impedance switch. Power transmitted across the transistor is in discrete pulses rather than as a steady current flow.

*By using suitable switching loss reduction technique, the switching frequency can be increased so as to reduce the size and weight of the inductors and capacitors.

16. What is an opto-coupler IC? Give examples. (Remember) (MAY 2010) [MAY/JUNE 2014]

Opto-coupler IC is a combined package of a photo-emitting device and a photo sensing device. Examples for opto-coupler circuit: LED and a photo diode, LED and photo transistor, LED and Darlington. Examples for opto-coupler IC: MCT 2F, MCT 2E.

17. Mention the advantages of opto-couplers: **(Remember) [Apr/May 2021]**

*Better isolation between the two stages.
*Impedance problem between the stages is eliminated.
*Wide frequency response.
*Easily interfaced with digital circuit.
*Compact and light weight.
*Problems such as noise, transients, and contact bounce are eliminated.

18. What is an isolation amplifier? Mention it's application. (Remember) (MAY/JUNE 2010) [APR/MAY 2016]

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

19. What is the need for a tuned amplifier? (Remember) (MAY 2009)

In radio or TV receivers, it is necessary to select a particular channel among all other available channels. Hence some sort of frequency selective circuit is needed that will allow us to amplify the frequency band required and reject all the other unwanted signals and this function is provided by a tuned amplifier.

20. Give the classification of tuned amplifier: **(Remember)**

(i) Small signal tuned amplifier
*Single tuned
*Double tuned
*Stagger tuned
(ii) Large signal tuned amplifier.

21. Write the frequency of oscillation (f0) equation for triangular wave generator (Remember) . (MAY10)

f0=R3/4R1C1R2

22. How frequency to voltage converted on OP-AMPS. (Understand) (MAY 2010)

A Frequency to voltage converter produces an output voltage, whose amplitude is a function of frequency of the input signal. The input signal may be a sine wave, a square wave or a pulse train. The F/V converter is essentially an FM detector or discriminator.

23. What is video amplifier? (Remember)
(MAY/JUNE 2010)

The video or wideband amplifiers are designed to provide a relatively flat gain versus frequency response characteristics for the range of frequencies required to transmit video information.

24. Define Multivibrators. Mention its types. (Remember)[APR/MAY 2019] (MAY/JUNE 2010) [MAY/JUNE 2014]

Multivibrators are regenerative circuits, which are mainly used in timing applications. Based on their operational characteristics they can be classified into

- •AstableMultivibrators
- •MonostableMultivibrators
- • BistableMultivibrators

25. Define AstableMultivibrators. (Remember)

The astableMultivibrators toggles between one state and the other without the influence of any other external control signal. It is also called as free running multivibrator.

26. Define MonostableMultivibrators(Remember)

The monostablemultivibrator or one –shot requires an external signal called a trigger to force the circuit into a quasi-stable state for a particular time or delay.

27. What is audio amplifier? (Remember)

The amplifier receives an input from signal source or from a transducer and gives out an amplified signal to the output device is called an audio amplifier.

28. Define AstableMultivibrators. (Remember)

The astableMultivibrators toggles between one state and the other without the influence of any other external control signal. It is also called as free running multivibrator.

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30. What is audio amplifier? (Remember)

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31. What are the three different wave forms generated by ICL8038? (Remember)

[APR/MAY 2010]

Sine wave, Square wave & Triangular wave.

32. What is meant by thermal shutdown applied to voltage regulators? (Remember)

[NOV/DEC 2010]

The IC has a temperature sensor which turns off the IC when it becomes too hot. The output current will drop and remain there until IC has cooled significantly.

33. What is an opto-coupler IC? Mention its applications. (Remember) [APR/MAY 2011]

It is combined package of LED and Photodiode.

34. Define the duty cycle in Astablemultivibrator using IC 555. (Remember) [APR/MAY 2011]

Duty cycle = $(R_b / R_a+2R_b)*100$

35. What are the limitations of three terminal regulators(Remember) [APR/MAY 2012]

1. No short circuit protection.

2. Output voltage is fixed.

36. What is switched capacitor filter. (Remember) [NOV/DEC 2013]

A switched capacitor filter is a three terminal element which consists of capacitors, periodic switches and op-amps whose open circuit voltage transfer function represents filter characteristics.

37. Give the formula for period of oscillations in an op-amp as table circuit. (Remember)

[May/June 13]

$T = 2RC \ln(1+\beta / 1-\beta)$

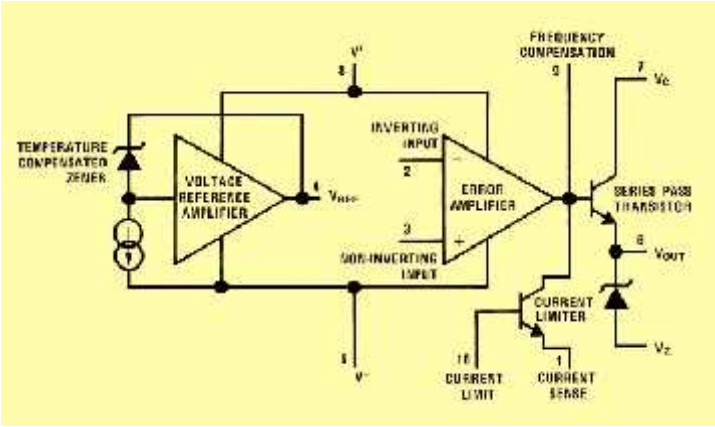
38. Define duty cycle of a periodic pulse wave form. (Remember) [May / June 2013]

Duty cycle = (Rb / Ra+2Rb)*100

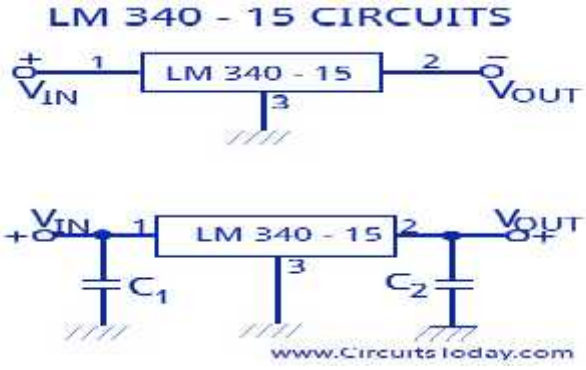
39. State the two conditions for oscillations? (Understand) [APR/MAY 2015]

1. The loop gain is equal to unity in absolute magnitude and
2. The phase shift around the loop is zero or an integer multiple of 2π

40. Draw the functional diagram of 723 regulator?(Apply) [NOV/DEC 2018] [APR/MAY 2015]



41. What is the purpose of connecting a capacitor at the input and the output side of an IC voltage regulator? (Remember) [NOV/DEC 2015]



The figure above shows the application of LM340 IC as a voltage regulator. Pins 1, 2, and 3 are the input, output and ground.

When there is quite a distance (in cms) from the IC to the filter capacitor of the unregulated power supply, there may occur unwanted oscillations within the IC due to lead inductances within the circuit. In order to remove this unwanted oscillation, the capacitor C1 has to be placed as shown in the circuit. Capacitor C2 is sometimes used to improve the transient response of the circuit.

Any device in the LM 340 series needs a minimum input voltage at least 2 to 3 V greater than the regulated output voltage. Otherwise, it will stop regulating. Furthermore, there is a maximum input voltage because of excessive power dissipation.

42. Mention two applications of frequency to voltage converter. (Remember) [NOV/DEC 2015]

1. Frequency to voltage converter in tachometers.
2. Frequency difference measurement.

43. Write the advantages of switching regulator over series voltage regulators. (Remember) [R2008 NOV/DEC 2015]

	Linear regulator	Switching regulator
Buck Boost Buck/Boost Inverting	Possible Impossible Impossible Impossible	Possible Possible Possible Possible
Effciency	V_O/V_{IN} Mostly low	Approx. 95% Usually high
Output power	Generally several watts Depending on thermal design	Large power possible
Noise	Low	Switching noise exists
Design	Simple	Complicated
Parts count	Low	High
Cost	○	△

44. List any two features of a fiber optic IC. (Remember) [R2008 NOV/DEC 2015]

45. A Hartely oscillator L1=10mH, L2=5mH and C=200pF.Calculate the frequency oscillation. (Apply) [APR/MAY 2016]

$fr=1/2\pi\sqrt{(L_TC)}$

$L_T=L1+L2=15mH$ fr =91.93 kHz

46) Draw the block schematic of IC 555 timer. (Remember) (Nov / Dec 2016)

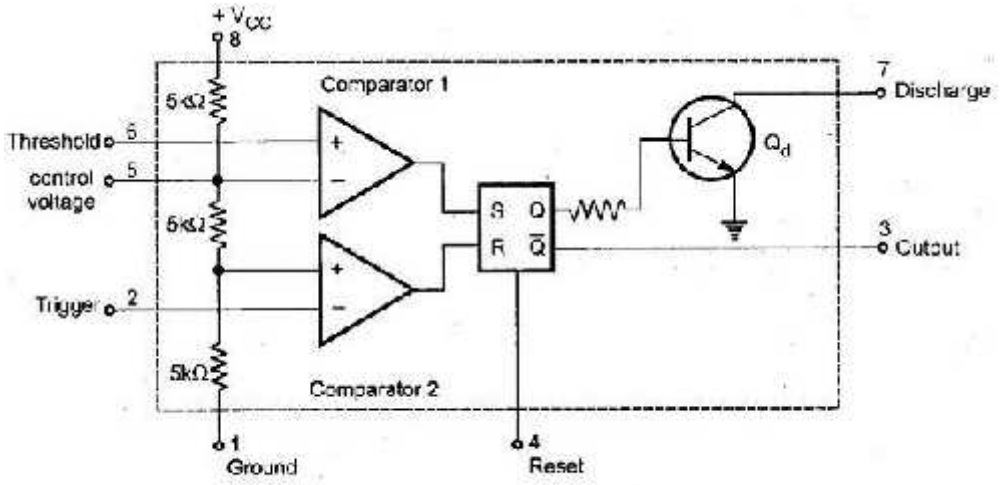


Fig. 2.100 (b) Block diagram of IC 555 timer

47) What is the function of a voltage regulator (Remember) (Nov / Dec 2016)

The purpose of a voltage regulator is to keep the voltage in a circuit relatively close to a desired value. Voltage regulators are one of the most common electronic components, since a power supply frequently produces raw current that would otherwise damage one of the components in the circuit.

48) **Distinguish the principle of linear regulator and a switched mode power supply. (April/May 2017) (Understand)**

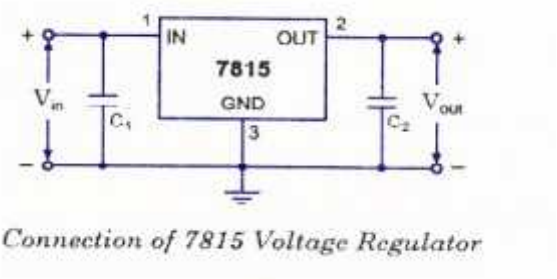
A switching power supply operates by constantly switching the source on and off; the rate of which is dictated by the needed voltage at the output. A linear power supply is often used because of its simplicity. Linear regulators exist in packaged ICs that only need a rectified voltage source to operate.

49) Define current transfer ratio of an opto-coupler?[Nov/Dec 2017](Remember)

The current transfer ratio refers to the ratio of the output collector current (Ic) to the input forward current(I_f)

CTR ={Ic/I_f }*100

50) Draw a fixed voltage regulator circuit and state its operations?[Nov/Dec 2017](Remember)



Connection of 7815 Voltage Regulator

51)Name some LC oscillator circuits. [APR/MAY 2015] (Remember)

Hartley Oscillator

Colpitts Oscillator

52) List the applications of multivibrator? ?[Nov/Dec 2018](Remember)

Frequency divider

Pulse width Modulation

Linear ramp generator
Square wave generator
VCO
Schmitt trigger

53)State the function of optocoupler. **[APR/MAY 2019] (Remember)**

Optocoupler provides electrical isolation between two circuits.

PART - B

1. Explain in detail the function of 555 timer in astable mode and derive the expression for frequency of oscillation. (Understand) [Nov'06]
2. Explain in detail the function of 555 timer in monostable and derive the expression for frequency of oscillation. (Analyze) [APR/MAY 2015]
3. Draw the internal functional diagram of 555 timer and explain briefly about each pin. (Apply) [May'03]
4. a) Draw and explain the astable operation using 555 to achieve 50% duty cycle and derive the expression for the frequency of Oscillation. (Apply)
   b) Write short notes on Optocouplers? (Remember) (Nov/ Dec 2016)
5. Design a adjustable voltage regulator using IC 723 to obtain positive low voltage and high voltage. (Analyze) [APR/MAY 2015]
6. Explain briefly about [Nov'07]
   (a) Power amplifiers (5)
   (b) Tuned amplifiers (5)
   (c) Video amplifiers (6) [APR/MAY 2019]
7. Draw & explain the internal diagram of IC LM723 voltage regulator. [ECENov'07] (Understand)
8. With necessary diagrams explain the operation and applications of LM380 IC. [EEE May'08] (Understand)
9. Explain the current limiting and current boosting feature of IC LM723. (Understand)
10. With neat diagram explain the working of step down switching regulator. [ECE Jun'06] (Understand)
11. Explain about the function generator using IC 8038. [APR/MAY 2015] (Understand)
12. Explain about opto coupler. What are its advantages? (Understand)
13. Draw & explain the internal diagram of IC LM317 voltage regulator. (Understand)
14. Draw and explain the principle of saw tooth generator. (Understand) [Apr/May 2018] [NOV/DEC 2018]
15. Draw and explain the operation of a triangular wave generator. [APR/MAY 2015] [NOV/DEC 2018] (Understand) [APR/MAY 2019] [Apr '11]
16. With suitable diagram, explain the working of a switched capacitor filter. Also explain how resistor can be realized using switched capacitor filter. (Understand) **.[APR/MAY2021]** [Apr '11]
17. With necessary diagrams, explain the operation of frequency to voltage converter.(Understand) [Apr '11]
18. With a neat diagram, explain the working of step down switching regulator. (Understand) [Apr '11]

19.(i) How is voltage regulators classified? Explain a series voltage regulator. (Understand)

(ii) What is an optocoupler? Briefly explain its characteristics. (Understand) [APR/MAY 2010]

20.(b) With a neat circuit diagram and internal functional diagram explain the working of 555 timers in astable mode. (Understand) [APR/MAY 2010]

21. (i) How can the current drive capability be increased while using three terminal voltage regulators? (Understand) [NOV/DEC 2010]

(ii) Design an adjustable voltage regulator circuit using LM317 for the following specifications: (Analyze)

Input dc voltage = l3.5 V
Output DC voltage = 5 to 9 V
Load current (maximum) =1 A

22. Describe the working of IC723 voltage regulator and explain how it can be used as high voltage regulator**.[APR/MAY2021]** (Understand) [NOV/DEC 2010]

23. Sketch the functional block diagram of the following and explain their working principle
(i) IC555 Timer (ii) General purpose voltage regulator (Understand)
[NOV/DEC 2013] [MAY/JUN 2012]

24.(i)Explain the working principle of isolation amplifier. (Understand) (Nov/ Dec 2016) [NOV/DEC2013][MAY/JUN 2012]

(ii) Explain the principle of operation of optocouplers . (Understand) [Apr/May 2018][NOV/DEC 2013]

25. State the advantages of IC voltage regulator. Explain the features and internal structure of general purpose Linear IC 723 Regulator. Design a regulator using IC 723 to meet the following specifications: Vo = 5V, Io = 100 mA, Vin = 15 $\pm$ 20 %, Isc = 150 mA, Vsense = 0.7V.
(Analyze)[May/June 2013]

26. Write detailed notes on the following (Remember)

i) Low noise op-amps.

ii) Integrated Fiber optic system. [May / June 2013]

27. Explain the working of Monostable Multivibrator. (Understand)

[APR/MAY 2015][NOV/DEC 2013]

28. Describe the operation of astable multivibrator using op amp. (Understand)
[NOV/DEC 2014]

29. Explain the operation of switching regulator using op-amp. (Understand)
[NOV/DEC 2014]

30. Briefly describe monolithic switching regulators. (Understand) [APR/MAY 2015]

31. Design a phase shift oscillator to oscillate at 100Hz (Analyze) [APR/MAY 2015]

32. Describe monostablemultivibrator with necessary diagrams and derive for ON time and recovery time. (Understand) [APR/MAY 2015]

33. With a neat functional diagram, explain the working of 555 timer as monostable multivibrator and derive an expression for the frequency of oscillation with relevant waveforms. (16) (Apply) [NOV/DEC 2015]

34. With a neat circuit diagram, explain the working of voltage regulator using operational amplifier .(16) . (Understand) [NOV/DEC 2015]

35. Draw the functional diagram for a low voltage regulator using IC723 and explain its operation. (8) (Understand) [R2008NOV/DEC 2015] [NOV/DEC 2017]

36. State the production circuit used in voltage regulators and explains them with characteristic curve. (8) (Understand) [R20008 NOV/DEC 2015]

37. Describe the astable mode of operation of IC555 timer and discuss any two applications. (8) (Understand) [R2008NOV/DEC 2015]

38. Explain how opto-couplers can be used in circuits for isolation.(6) (Understand) [R2008NOV/DEC 2015]

39. Briefy write the working principle and functionalities of LM 380 audio amplifier. (8) (Understand) [APR/MAY 2016] [NOV/DEC 2017] [APR/MAY 2019]

40. Draw the schematic of a linear IC saw tooth waveform generator and explain the circuit operation (8) (Apply) [APR/MAY 2016]

41. Summarize the working principle of IC723 general purpose voltage regulator. (12) [APR/MAY 2016] (Understand)

42. A 555 timer is configured in as table mode with R_A =2k ohm R_B=6k ohm and C=0.1μF.Determine the frequency of oscillation. (4)(Apply) [APR/MAY 2016]

43) Discuss the functionalities and working of switched mode power supply (Nov/Dec 2016) (Understand)

44) Describe the 555 Timer IC. Design a Astable Multivibrater Circuit to generate output Pulses of 25%, 50% duty cycle using a 555 Timer IC, with choice of C = 0.01,uF, Frequency as 4.0 KHz (April May 2017) Create

45) Explain switched capacitor filter , audio power amplifier, opto coupler? (April May 2017) (Remember).

46) With neat diagram, explain the operation of an astable and monostable multivibrator [NOV/DEC 2017] (Understand) [NOV/DEC 2018]

47) Design a frequency to voltage converter using IC VFC 32 for a full scale output of 8 V for a full scale input frequency of 80 kHz with a maximum ripple of 8 mV. [NOV/DEC 2017] (Understand)

48) Design a square wave genorator using 555 timer for a frequency of l20 Hz and 60% dirty cycle. Assume C = 0.2 μF.[Nov/Dec 2017](Create)

49)State significant difference between Fixed and adjustable voltage regulators. [NOV/DEC 2018] (Understand)

50) Design a wave generator using 555 timer for a frequency of 110Hz and 80% duty cycle.Assume C= 0.16μF. .[Nov/Dec 2018](Create)

51)What are the modes of operation of a timer?Draw the functional diagram of a square wave generator using timer and derive its duty cycle. **.[APR/MAY2021](understand)**

ASSIGNMENT QUESTIONS

1.If an IC 555 timer is used to generate a Ramp voltage with constant collector current of 1 mA, Vcc=15V and C=0.1µF,What would be the slope of the ramp generated? How much is the peak value of the ramp generated? What is the duration of the Ramp? (PO1)(REMEMBER)

2. Design a square wave oscillator so that Fo= 1KHz.The op amp is IC741 with dc supply voltage ±15V. (PO3)(CREATE)

3. Design a triangular wave generator so that Fo= 2KHz and Vo = &Vpp. The opamp is IC1458/772 and supply voltages are ±15V. (PO3)(CREATE)

4. Using MF5 design a second order butterworth LPF with a cut off frequency of 500Hz and a passband gain of -2. Assume +5V power supply and CMOS clock (PO3)(CREATE)

5. How a monostable multivibrator can be used as a divide by 2 network considering the frequency of input trigger as 2 KHz. (PO1)(REMEMBER)

6. Design an adjustable voltage regulator to satisfy the following specifications. Use LM317 regulator. Output voltage Vo = 5-12 V, Output current Io = 1 A. (PO3)(CREATE)

7. The teletypewriter uses the frequencies 1070Hz and 1270 Hz for its MODEM. Design the FSK generator circuit for this application. (PO3)(CREATE)

8. Using opamp design a phase shift oscillator to oscillate at 100Hz. (PO3)(CREATE)

9. Design a timer which should turn on heater immediately after pressing a push button and should hold heater in ON state for 6 Seconds. (PO3)(CREATE)

10. Design an Astable multivibrator circuitwhich will flash the electric bulb such that its on time will be 4 seconds and off time will be 2 Seconds. (PO3).(CREATE)