EC8095
VLSI DESIGN

EC8095-VLSI DESIGN

UNIT I INTRODUCTION TO MOS TRANSISTOR

MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.

UNIT II COMBINATIONAL MOS LOGIC CIRCUITS

Circuit Families: Static CMOS, Ratioed Circuits, Cascade Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. Power: Dynamic Power, Static Power, Low Power Architecture.

UNIT III SEQUENTIAL CIRCUIT DESIGN

Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. Timing Issues: Timing Classification Of Digital System, Synchronous Design.

UNIT IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff. Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

UNIT V IMPLEMENTATION STRATEGIES AND TESTING

FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

TEXT BOOKS:

1. Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective‖, 4th Edition, Pearson , 2017 (UNIT I,II,V)

2. Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective‖, Second Edition , Pearson , 2016.(UNIT III,IV)

REFERENCES

1. M.J. Smith, —Application Specific Integrated Circuits‖, Addisson Wesley, 1997

2. Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition McGraw Hill Education,2013

3. Wayne Wolf, —Modern VLSI Design: System On Chip‖, Pearson Education, 2007 4. R.Jacob Baker, Harry W.LI., David E.Boyee, —CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.

COURSE OUTCOME:

CO1	Knowledge about the MOSFET basics, operation, characteristics and layout design rules for CMOS fabrication.
CO2	An ability to compute delay in digital circuits and analyze the effect of power dissipation and design knowledge about the different types of circuit families.

CO3	Knowledge about the different types of latches, registers and memory control circuits and their appropriate applications in designing of digital circuits.
CO4	An ability to design arithmetic circuits with low speed, area etc
CO5	Knowledge about the FPGA building block architecture routing procedures for chip design.
CO6	Knowledge about the testers, test programs and design for testability.

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PART A

1. What are the advantages and disadvantages of SOI process? (Understand)

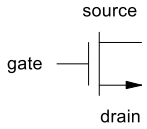
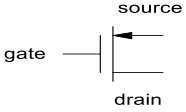
Advantages:

- There is no well formation in this process.
- There is no field inversion problem
- There is no body effect problem.

Disadvantages:

- It is very difficult to protect inputs in this process.
- Device gain is low.
- The coupling capacitances between wires always exist.

2. Distinguish b/w NMOS and PMOS devices?(Understand)

nMOS	pMOS
	
In nMOS, electrons are the majority carriers. When positive voltage is applied on gate, no of electrons will increase. So conductivity of channel is increased	In pMOS, majority carriers are holes.
Switching speed is high, since the mobility of electron is high.	Switching speed is low, since the mobility of hole is low.
nMOS conducts at logic 1.	pMOS conducts at logic 0.

3. What is meant by body effect? (Remember) [MAY '2011,NOV 2016][April2020]

V_t is not constant with respect to voltage difference between substrate and source of transistor. This is known as body effect. It is otherwise known as substrate-bias effect.

4. What is velocity saturation? (Remember) May 2018

The saturation current increases less than quadratic ally with increasing V_{gs} .Tis is caused by two effects velocity saturation and mobility degradation. At high electric fields strengths V_{ds}/L carrier velocity ceases to increase linearly with field strength. This is called velocity saturation and results in lower I_{ds} ,than expected at high V_{ds}.

5. Define inversion layer? (Remember)

When a higher positive potential greater than critical threshold is applied, it attracts more positive charge to the gate. These holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This conductive layer of electrons in the p-type body is called inversion layer.

6. Define noise Margin? (Remember)(April 2020)

Noise margin represents the amount of noise voltage on the input of a gate so that the output will not be corrupted. It is closely relate to the dc characteristics. and it is also known as noise immunity.

There are two parameters

- Low noise margin-NM_L
- High noise margin-NM_H

7. Give the expression for rise time and fall time in cmos inverter circuit.(Apply)

[NOV '2011]

Rise time:

The time needed for v_{out} to rise fron 0.1 v_{dd} to 0.9 v_{dd} is called rise time.

$t_r = \ln(9)\ \tau_p$

$t_r = 2.2\ \tau_p$

Fall time:

The time needed for v_{out} to fall from 0.9 v_{dd} to 0.1 v_{dd} is called fall time.

$t_f = \ln(9)\ \tau_n$

$t_f = 2.2\ \tau_n$

8. What are the steps involved in manufacturing of IC? (Remember)

The steps are

- Wafer preparation
- Epitaxial growth
- Oxidation
- Photo lithography
- Diffusion and Ion implantation

- Isolation
- Metallization

9. What is photo lithography? (Remember)

The patterning is achieved by a process called photolithography. In areas where the mask is absent, the implantation can occur, or dielectric or metal could be etched away.

10. What is isolation? (Remember)

It is process used to provide electrical isolation between different components and interconnections.

11. What is twin tub process? Why it is called so? (Understand)

Twin Tub process is one of the CMOS technologies. There are two wells available in this process. The other name of well is tub. So because of these two tubs, this process is known as twin tub process. Here, threshold voltage, body effect of n and p devices is optimized.

Advantages:

- Separate optimized wells are available
- Balanced performance

12. What is stick diagram? (Remember)

The diagram which conveys the layer information through the use of colour is known as stick diagram.In this pMOS and nMOS transistors are separated by demarcation line.X is the symbol used to represent v_{dd} and vss.Demarcation line is imaginary. v_{dd} and vss lines are known as rails.

13. What are the two types of layout design rules? (Remember)

The two major types of layout design are

- Lambda design rule
- Micron rule

14. What are the 3-modes of n-MOS enhancement transistor? (Remember)

The three modes are

- Accumulation mode
- Depletion mode
- Inversion mode

15. What are the different regions in nMOS depending upon voltages?[MAY '2012] (Remember)

There are three different regions in nMOS transistor depending upon the operating voltages i.e V_{gs} &V_{ds}

- When $V_{gs}<V_t$ &V_{ds} =0-cut off region
- When $V_{gs}<V_t$ &V_{ds} <V_{gs}-V_t -Linear region
- When $V_{gs}<V_t$ &V_{ds} >V_{gs}-V_t -Saturation region
- Low noise margin-NM_L
- High noise margin-NM_H

16. Why the tunneling current is higher for NMOS transistors than PMOS transistors with silica gate? ?(Understand) NOV '2012

Tunneling current is an order of magnitude higher for nMOS than pMOS transistors with Sio_2 gate dielectrics because the electrons tunnel from the conduction band while the holes tunnel from thevalence band and see a higher barrier.

17. What is channel length modulation? (Remember) [Nov '2011][May 2016,May 2017]

The depletion layer increases at the drain as the drain voltage is increased. This leads to a shorter channel length and the drain current increases by a factor of $(1+\lambda V_{ds})$.This is called Channel length modulation.

18.What is mobility degradation? (Remember)

When the V_{gs} increases,it results in the strong vertical electric fields and this cause the carriers to scatter against the surface and also reduce the carrier mobility μ.This effect is called mobility degradation.

19.Define mobility. (Remember)

The mobility μ is defined as the ratio of average carrier drift velocity (V) to the electric field intensity (E)

$$\mu = \frac{Average\ carrier\ drift\ velocity\ (V)}{Electric\ field\ intensity\ (E)} \quad \frac{cm^2}{V-sec}$$

20.What is drain punchthrough? (Remember)

When the drain is at a high enough voltage with respect to the source,the depletion layer around the drain and source regions merge into a single depletion region thus causing to flow irrespective of the gate voltages.This is known as a punchthrough effect.

21.What is latch up condition in CMOS circuits? (Remember) May 2016

Latch-up is a condition which creates a short circuit from positive supply voltage to ground. Latch –up is a condition occurs when:

(i) The parasiticc components give rise to the establishment of low resistance conducting path between VDD and GND

(ii) The product of the gains of the two transistor (n & p) in the feedback loop, $b_1 * b_2$ is greater than one.

22.What are the system approaches to prevent Latch-Up? ?(Understand) May 2016

- By using proper grounding technique.
- By using decoupling capacitors at the supply pins of the IC.
- By placing a reverse biased diode between each supply rail and the I/O pins
- By placing series resistance to limit the fault current to a safe value.
- Carefully protect electrostatic protection devices associated with I/O pads with guard rings
- Reduce the gain product $b_1 * b_2$
- Reduce the well and substrate resistances.

23.What is Design Rule? (Remember)

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. The design rule conform to a set of geometric constraints or rules specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon interconnects or diffusion area, minimum feature dimensions and minimum allowable separations between two layers.

24. What is Micron design rule? (Remember) May 2014

Micron rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

25.What is Lambda design rule? (Remember) [MAY '2013],NOV '2012, May 2014

Lamda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter λ and thus allow linear proportional scaling of all geometrical constraints. λ is generally half of the minimum drawn transistor channel length.This length is the distance between the source and drain of a transistor and is set by the minimum width of a polysilicon wire.

26.What is accumulation mode? (Remember)

When the gate to source voltage (V_{gs}) is much less than the threshold voltage (V_t) then there is no conduction band between source and drain.The device is terned off.This mode is termed as accumulation mode.

27.What is depletion mode? (Remember)

When the gate to source voltage (V_{gs}) is raised above than the threshold voltage (V_t) then the electrons are attracted towards the gate while the holes are repelled causing a depletion region under the gate.This mode is termed as depletion mode.

28.What is inversion mode? (Remember)

When the gate to source voltage (V_{gs}) is much greater than the threshold voltage (V_t),the electrons are attracted to the gate region.Under such a condition the surface surface of the underlying p-type silicon is said to be inverted to n-type,and provides a conduction path between source and drain .This mode is termed as inversion mode.

29. What are the NON-ideal IV effects? (Remember) MAY 2014

- channel length modulation
- Body effect
- Velocity saturation
- Mobility degradation

30.Define Low Noise Margin N_{ML}. (Remember)

The Low Noise Margin N_{ML} is defined as the difference in magnitude between maximum low input voltage of the driving gate and the maximum output low voltage recognized by the driven gate. Thus $\mathbf{N_{ML} = |V_{ILMAX} - V_{OLMAX}|}$

31. Define High Noise Margin N_{MH}. (Remember)

The Low Noise Margin N_{ML} is defined as the difference in magnitude between maximum low input voltage of the driving gate and the maximum output low voltage recognized by the driven gate.Thus

$$\mathbf{N_{MH} = |V_{OHMIN} - V_{IHMIN}|}$$

32. What are the main four CMOS technologies? (Remember)

- N-well process
- P-well process
- Twin-tub process ,Silicon on Insulator

33. What is CMOS technology? (Remember)

Complementary Metal Oxide Semiconductor (CMOS) in which both n-channel MOS and p-Channel MOS are fabricated in the same IC.

34. What are the advantages of CMOS technology? ?(Understand)

- Low power consumption
- High performance
- Scalable threshold voltage
- High noise margin
- Low output drive current

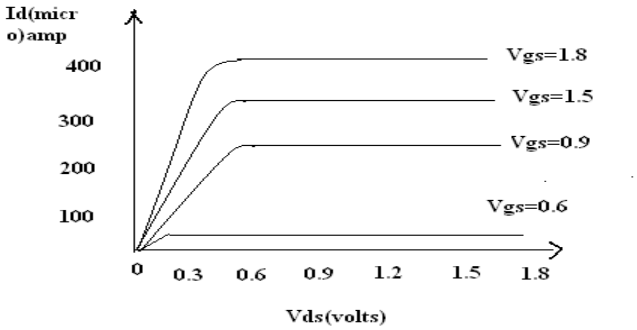
35. What are the disadvantages of CMOS technology? ?(Understand)

- Low resistance to process deviations and temperature changes.
- Low switching speed at large values of capacitive loads.

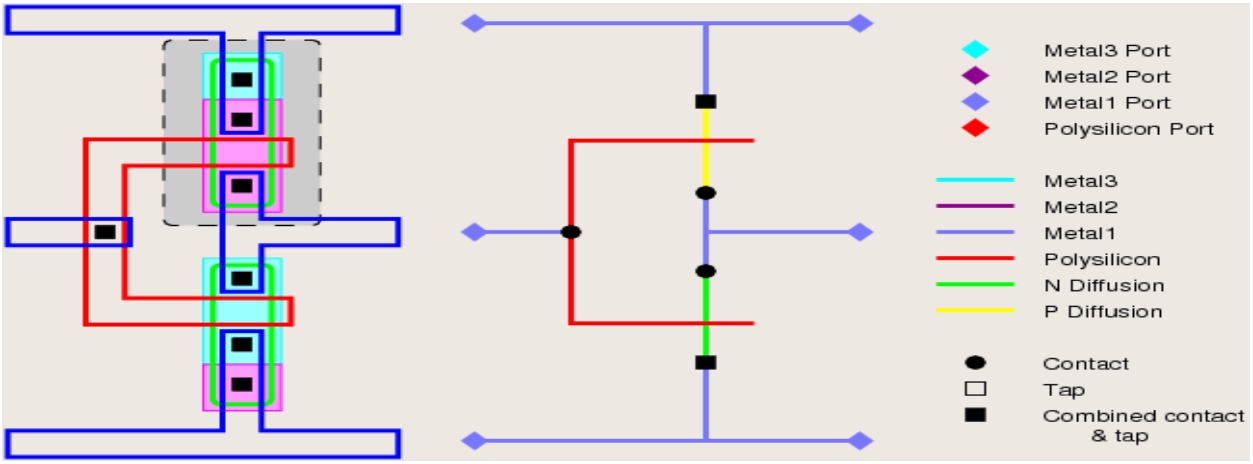
36. What are the advantages of CMOS technology over NMOS technology? (Understand)

- In CMOS technology the aluminum gates of the transistors are replaced by polysilicon gate
- The main advantage of CMOS over NMOS is low power consumption.
- In CMOS technology the device sizes can be easily scalable than NMOS.

37. Draw the ideal IV characteristics of NMOS transistor. (Remember) [MAY '2012]



38.Draw the stick diagram and layout for CMOS Inverter.(Apply) NOV 2016



39.List the scaling principles(Remember) May 2018

Scaling is a proportional adjustment of the dimensions of an electronic device while maintaining the electrical properties of the device, results in a device smaller than the un-scaled device.

Scale the devices and wires down, make the chips 'fatter' in-functionality, intelligence, memory and faster, make more chips per wafer and increased yield. The only constant in VLSI design is constant change. Feature size has reduced by 30% every two to three years. As transistors become smaller, they switch faster, dissipate less power, and are cheaper to

manufacture. However, scaling also exacerbates reliability issues, increases complexity, and introduces new problems.

40.Why nMOS transistor is selected as a pull down transistor.(Understand) Nov 2017

In CMOS inverter , pull up is nMOS transistor and pull down is pMOS transistor. When logic 1 is applied as input, nMOS transistor turns ON and PMOS transistor turns OFF. Hence, the output should get charged to V_{dd}. But due to threshold voltage effect, nMOS is not capable of passing Vdd/ good logical 1 at the output.

Hence, the output will be Vdd-Vth.When logic 0 is applied as input, nMOS transistor turns OFF and PMOS transistor turns ON. Hence, the output should get discharged to ground level. But due to threshold voltage effect, pMOS is not capable of passing good logical 0 at the output. Hence, the output will be 0-|Vth|.

Thus, in order to obtain good logic 0 and logic 1 output, always pull up devices are PMOS and pull down devices are NMOS.

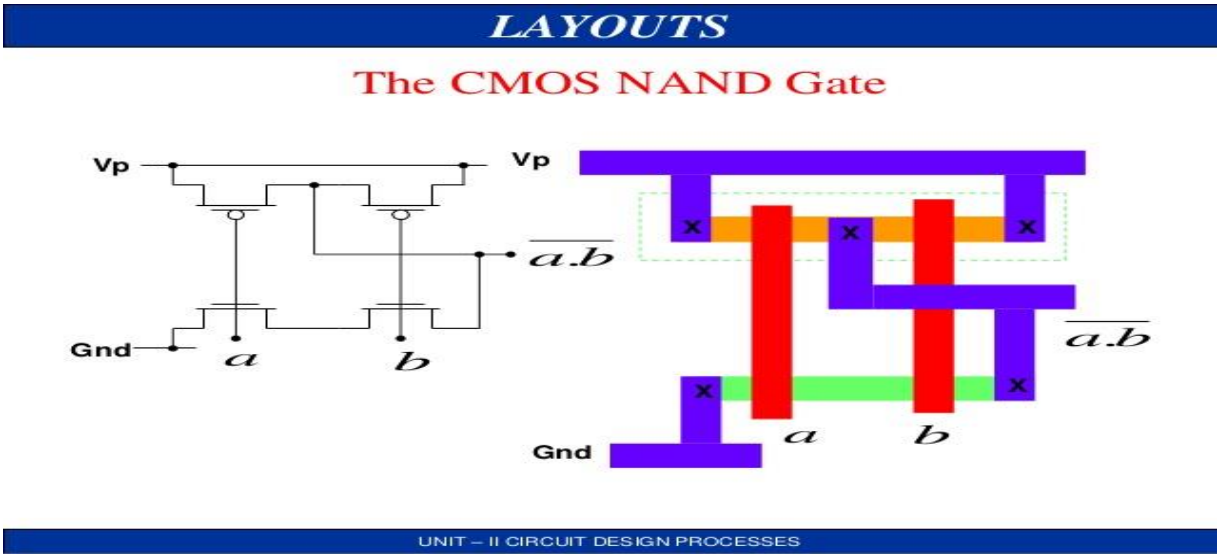
41.What is the need of demarcation line? (Remember) Nov 2017

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS transistor must lie on one side of the line and all nMOS transistor will have to be on the other side.

42. Why NMOS device conducts strong zero and week one? Nov/dec2018.(Understand)

So the maximum voltage level that the output node can be charged to is VDD-Vthn. So the maximum voltage level that the output node can be discharged to is |Vthp|. So an **NMOS** passes **weak 1** and PMOS passes **weak 0** whereas no such situations occur when an **NMOS** passes **0** and a PMOS passes **1**.

43. Draw the stick diagram of static CMOS 2 input NAND gate. Nov/Dec2018.(Understand)



44. Define the threshold voltage of MOSFET. **(Remember) April/May 2019**

Threshold voltage is the **voltage** applied between gate and source of a **MOSFET** that is needed to turn the device on for linear and saturation regions of operation. The following analysis is for determining the **threshold voltage** of an N-channel **MOSFET** (also called an N-**MOSFET**).

45. By what factor, gate capacitance must be scaled if constant electric field scaling is employed. **(Understand) April/May 2019**

Scaling Factors -1

Explanation: Constant electric **scaling model** and constant voltage **scaling model is used for scaling**. Explanation: α is **used** as the **scaling** factor for linear dimensions where as β is **used** for supply voltage V_{dd}, gate oxide thickness etc.

PART B

1. Explain n-well/ nMOS transistor process with neat diagrams? **(Understand)**

MAY '2012/NOV '2011, NOV '2012, NOV 2016

2. Explain the working principle of n-MOS enhancement transistor with various modes of operation. **(Understand)**

3. Explain the regions of DC characteristics of CMOS inverter.N**OV '2011MAY '2012, NOV '2012, [MAY '2013], May 2014, May 2015, May 2016,May 2017**

(Analyze)

4. Explain in detail about the ideal I-V characteristics and non-ideal I-V characteristics of NMOS and PMOS devices **(Analyze) [MAY '2013] [Nov 2021]**

5. Derive the expression for current in nMOS transistor in different regions. **(Apply) May 2016, MAY '2011, NOV 13**

6. Explain the capacitance model of nMOS transistor. **(Understand) MAY '2012**

7. Write in detail about the layout design rules. **(Understand) MAY '2011, May 2014**

8. Write short notes on (i) Noise Margin and Effect of β_n / β_p ratio in DC characteristic curve of CMOS Inverter. **(Understand) NOV 2016**

9. Discuss in detail about CMOS inverter layout design rules.**(Understand)MAY '2012,NOV 2016**

10.

An NMOS transistor has the following parameters : gate oxide thickness = 10 nm, relative permittivity of gate oxide = 3.9, electron mobility = 520 cm^2/V-sec, threshold voltage = 0.7 V, permittivity of free space = 8.85×10^{-14} F/cm and (W/L) = 8. Calculate the drain current when (V_{GS} = 2 V and V_{DS} = 1.2 V) and (V_{GS} = 2 V and V_{DS} = 2 V) and also compute the gate oxide capacitance per unit area. Note that W and L refer to the width and length of the channel respectively.

NOV '2011(Apply)

11.
An NMOS transistor has a nominal threshold voltage of 0.16 V. Determine the shift in threshold voltage caused by body effect using the following data. The nMOS transistor is operating at a temperature of 300°K with the following parameters : gate oxide thickness (t_{ox}) = 0.2×10^{-5} cm, relative permittivity of gate oxide (ε_{OX}) = 3.9, relative permittivity of silicon (ε_{Si}) = 11.7, substrate bias voltage = 2.5 V, intrinsic electron concentration (Ni) = 1.5×10^{10} / cm^3, impurity concentration in substrate (N_A) = 3×10^{16} / cm^3. Given Boltzmann's constant = 1.38×10^{-23} J/°K, electron charge = 1.6×10^{-19} Coulomb and permittivity of free space = 8.85×10^{-14} F/cm. (8)

NOV '2012(Apply)

12. Derive the expression for rise time, fall time and propagation delay of CMOS inverter.**(Apply)** **May 2015**

13.Explain in detail about Body effect and its effect in device. **(Analyze)** **May 2016**

14.Discuss the principle of constant field and lateral scaling. Write the effects of the above scaling methods on the device characteristics. **(Analyze)** **Nov 2017,May 2016,May 2017**

15. Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors. **(Understand)** **NOV 2016**

16. Write the layout design rules and draw the layout of NAND and NOR Gate.**(Apply)** **Nov 2017,May 2017,May 2018**

17. Explain the dynamic behavior of MOS transistor with neat diagram. **(Understand)May 2018**

18. Explain the electrical properties of CMOS. **(Understand)** **Nov 2017**

19. List out the goals of CMOS technology scaling. Explain how common electric field scaling is superior than constant voltage scaling. **Nov/ Dec 2018. (Understand)**
20. Derive the expression to obtain the minimum delay through the chain of CMOS inverter. **Nov/ dec 2018(Apply)**
21. Explain the design techniques that are used for larger fan-in devices to reduce delay. **Nov/ Dec 2018.(Understand)**

22. Draw the small signal model of device during cut-off, linear and saturation region. **Nov/ Dec 2018(Understand)**

23. Derive an expression for Ids of nMOS in linear and saturated region **(Apply) April/May 2019**

24. Draw a CMOS inverter. Analyze the switching characteristics during rise time when

V_{in} changes from high to low. **(Understand)April/May 2019**

25. Draw the stick diagram of CMOS inverter. **(Understand)April/May 2019**

26. State the minimum width and minimum spacing lambda-based design rules to draw the layout. **(Understand)April/May 2019**

27.Draw and explain the equivalent RC circuit for an inverter. **(Understand) April/May 2019**

28. a) i) Differentiate static and dynamic latches and registers.

ii) Obtain the first-order model relating the current and voltage for an NMOS transistor in three regions of MOS operation. **(Understand)April/May 2020**

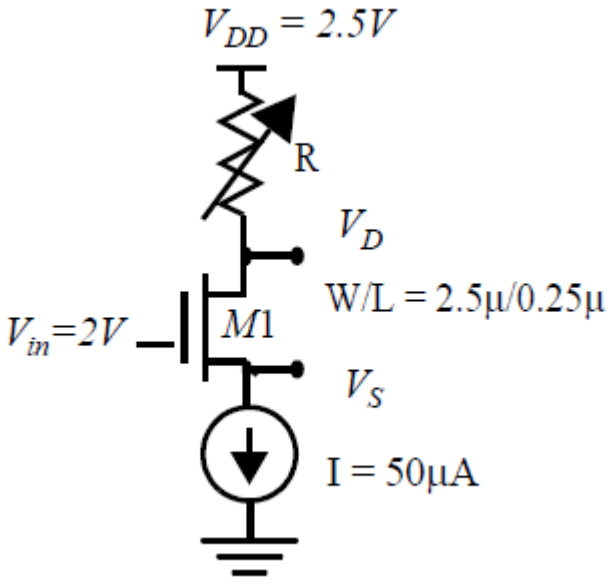
29. i) Explain the DC transfer characteristics of CMOS inverter.

ii) Estimate the delay of CMOS logic gates as the RC product of the effective driver resistance and the load capacitance. **(Understand)April/May 2020**

30.i) Differentiate static and dynamic power in CMOS circuits. ii) Sketch the 4:1 multiplexer using transmission gates. **(Understand)April/May 2020**

Assignment Questions:

1. With neat sketches, explain CMOS fabrication using Twin Tub Process. **(Apply)**
2. Derive the drain characteristic equation of a PMOS transistor. **(Apply)**
3. An NMOS device is plugged into the test configuration shown below in Figure.
The input *Vin* =2V. The current source draws a constant current of 50 μA. *R* is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences Short channel effects and has following transistor parameters: $k' = 110*10^{-6}$ V/A^2**,** VT = 0.4 , and VDSAT = 0.6V. The transistor has a W/L = 2.5μ/0.25μ. For simplicity body effect and Channel length modulation can be neglected. i.e λ=0, γ=0. .
   a. When *R* =10kΩ find the operation region, VD and VS.
   b. When R= 30kΩ again determine the operation region VD, VS
   c. For the case of R = 10kΩ, would VS increase or decrease if $\lambda \neq 0$. Explain qualitatively



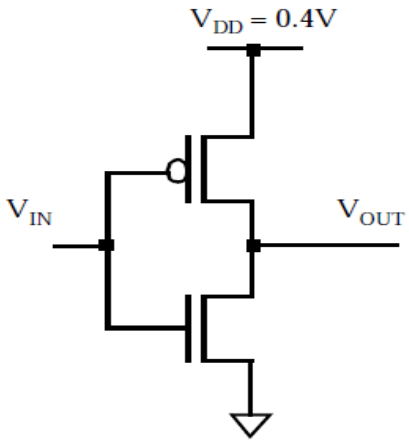
(Analyze)

4. Consider an NMOS transistor with the following parameters: tox = 6 nm, L = 0.24 µm,W =0.36 µm, L D = LS = 0.625 µm, CO = 3×10^{-10} F/m,C j0 = 2×10^{-3} F/m2, C jsw0 =2.75×10^{-10}F/m. Determine the zero-bias value of all relevant capacitances. **(Apply)**

5. Explain the term Latch up in CMOS Configuration and the techniques to prevent it**. (Understand)**

6. The inverter below operates with VDD=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical I0 and n. **(Apply)**

a. Calculate the switching threshold (VM) of this inverter.
b. Calculate VIL and VIH of the inverter.



7. Explain the hot carrier effect**. (Understand)**

8. Consider the nMOS transistor in 180nm process with a nominal threshold voltage of 0.4v and doping level of 8x1017cm-3.Propose the body voltage**. (Apply)**

UNIT II COMBINATIONAL LOGIC CIRCUITS

Circuit Families: Static CMOS, Ratioed Circuits, Cascade Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. Power: Dynamic Power, Static Power, Low Power Architecture.

PART –A

1.Give the classification of CMOS circuits. (Remember)

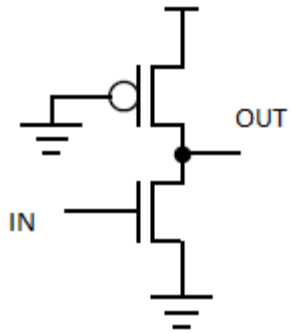
There are various CMOS logic circuits.They are
(i)Static CMOS logic
(ii)Ratioed Logic
- (a) Pseudo NMOS logic
- (b) Differential Cascode Voltage Switch Logic

(iii) Pass transistor Logic
(iv)Dynamic logic.

2.What is staic CMOS logic? (Remember)

Static CMOS logic is a combination of two networks ,Pull up Network using PMOS transistors and Pull down network using NMOS transistors.They are dual with each other.At any time ,any one of the network is on.

3.Sketch a pseudo NMOS inverter. (Remember) NOV 2011

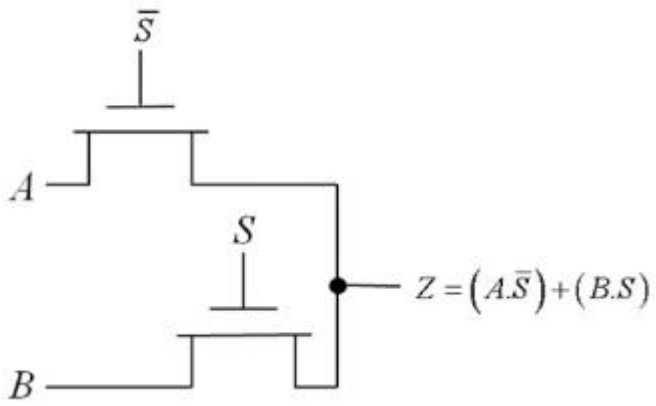


4.Write the expression for the logical effort and parasitic delay of n input NOR gate. Nov 2011 (Apply)

The logical effort of n input NOR gate is g= 2n+1/2
The parasitic delay of n input NOR gate is p=n

5.Implement a 2:1 multiplexer using pass transistor.(Apply)

If S=0; Z=A
S=1; Z=B



6.What is dynamic CMOS logic? (Remember)

Dynamic circuits reduce the drawbacks of ratioed circuits using a clock input to the pull up transistor(PMOS).It requires N+2 transistors and there are two modes of operation ,Precharge and Evaluation.

7.What are the disadvantages of dynamic logic? (Understand)

- Consume significant dynamic power
- Sensitive to noise during evaluation
- Carefull clocking
- Monotonicity problem

8.Why domino logic is preferred over dynamic logic? (Understand)

In dynamic logic ,there is cascading problem.This can be solved by placing a static – CMOS inverter between dynamic gates.The dynamic –static pair togethrer is called domino logic.

9.Define propagation delay. (Remember) May 2017

The propagation delay is the time taken to change the output after applying the input.This is the upper bound on interval between valid inputs and valid outputs.

10.Define Elmore Delay Model. (Remember) Nov 2017,May 2017,May 2018

The elmore delay model estimates the delay of an RC ladder as the sum over each node in the ladder of the resistance R_{n-I} between that node and the starting point ,multiplied by the capacitance on the node.

$t_{pd} = \sum_i R_{n-1} C_i = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$

11. What are the causes of static and dynamic power dissipation? (Understand) NOV 2016

- Static dissipation is due to

- Subthreshold conduction through off transistor
- Tunneling current through gate oxide
- Leakage current through reverse biased diodes
- Contention current in ratioed circuits

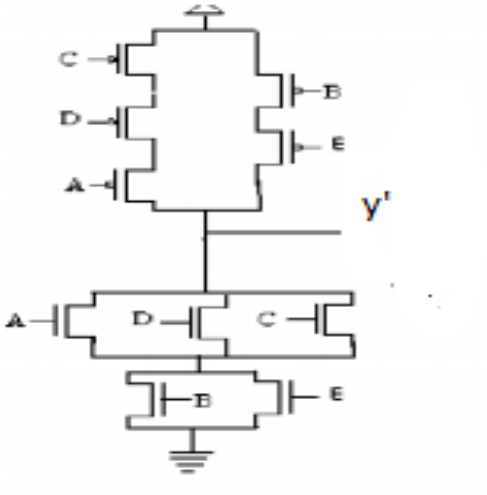
- Dynamic power dissipation is due to
  - Charging and discharging of load capacitances
  - Short circuit current while both PMOS and NMOS networks are partially on

12. What are the disadvantages of using a pseudo NMOS gate instead of a full CMOS gate? (Understand)

The NMOS size should be larger than pmos to make the output voltage $V_{OL} \approx 0$ .This in turn increase the time for charging the output node i.e slow rising transition.
There is static power dissipation when the output is low.

13.Implement the following function using CMOS logic. (Apply)

Y'=(A+D+C)(B+E)

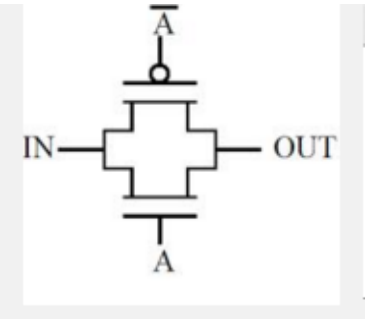


14.State any two criteria for low power logic design(Remember)

- The low power can be achieved by lowering the effective capacitance.This can be achieved by reducing the physical capacitance and switching activity.
- The non active modules can be made to stand by mode to reduce the power
- Multiple threshold CMOS circuits can be used .

15.What is transmission gate? (Remember)(April 2020)

Transmission gate is constructed by combining an NMOS transistor and PMOS transistor in parallel.It acts as a switch that turns on when a '1' is applied to the gate 'A'. When A=1,'0'and '1'can be passed strongly through IN.



16.What are the techniques to reduce switching activity? (Remember)

The switching activity can be reduced by the following techniques

- Logic restructuring
- Input ordering
- Time – Multiplexing resources
- Glitch reduction by balancing signal paths

17.Define logical effort. (Remember)

Logical effort of a gate is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current.

18.Give the expression of t_{PLH} and t_{pHL} of inverter with C_L.(Apply)

$t_{pHL} = 0.69 R_N C_L$

$t_{pLH} = 0.69 R_P C_L$

$t_P = (t_{pHL} + t_{pLH})/2$

19. Write the characteristics of DCVSL? (Remember)

DCVSL has the performance of radioed circuits without the static power consumption and provides rail-to rail swing. It uses both true and complementary input signals and computes both true and complementary outputs using a dual pair of NMOS pull down networks.

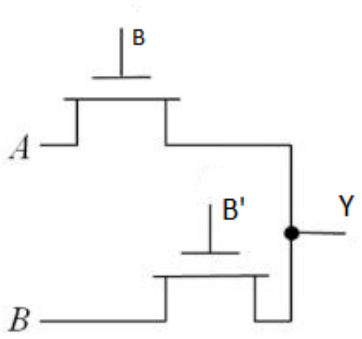
20. What is pass transistor logic? (Remember)

In pass transistor, the inputs are also given to source and drain terminals. This type of logic uses NMOS transistors alone. Pass transistor is a MOS transistor ,in which gate is driven by a control signal ,the source (out), the drain of the transistor is called constant or variable voltage potential (in) when the control signal is high, the input is passed to the output and when the control signal is low, the output is floating such topology circuit is called pass transistor.

21. Implement 2 input 'and' gate using pass transistor logic. (Apply)

A	B	Y
0	0	0
0	1	0

1	0	0
1	1	1



22. Give Elmore delay expression for propagation delay of an Inverter.

May 2016(Remember)

The Elmore delay expression for propagation delay of an Inverter is

T_p =0.69 RC.

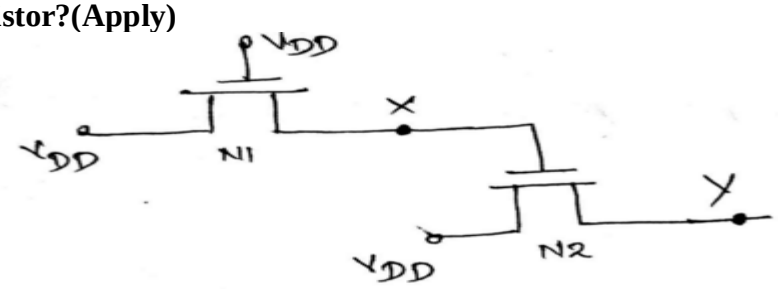
23. Why single phase dynamic logic structure cannot be cascaded? Justify. May 2016 (Understand)

The cascading problem arises because the output of each gate are pre charged to '1' and due to finite propagation delay Due to this, some charge will be loss and leads to reduced noise margin and potential malfunctioning.

24.State the advantages of transmission Gate? (Understand) May 2017

A CMOS transmission gate can be constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals.The main advantage of the CMOS transmission gate compared to NMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation

25.What is the value of Vout for the figure shown below ,where Vtn is threshold voltage of transistor?(Apply) NOV 2016



In the above figure,N1 output node X drives the gate of another transistor N2.Node X can charge upto VDD-Vtn1 only. Now the output Y charges upto X-Vtn2 i.e VDD-Vtn1-Vtn2.This shows the output is degraded.

26. List the types of power dissipation. (Remember) Nov 2017,May 2018 April 2020 (Understand)

There are two types of power dissipation
1. Static power dissipation
2. Dynamic power dissipation

29. State the various types of power dissipation. **(Understand)April/May 2019**.

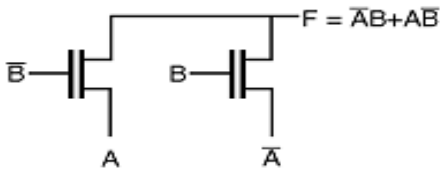
1. Static Power dissipation

2. Dynamic power dissipation

30. Draw a 2 input XOR using nMOS Pass transistor.**(Understand)April/May2019**

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Truth table of 'XOR' gate



'XOR' gate using pass transistor logic

PART-B

1. Explain about the Elmore Delay Model. **(Understand)**
2. Explain about Pseudo-NMOS gates with neat diagram. **(Understand) May 2011**
3. Derive and discuss in detail the characteristics of CMOS Transmission gate. **(Apply) Nov 2017,May 2011, May 2016,May 2017,May 2018**
4. Explain the static and dynamic power dissipation in CMOS circuits with expressions. **(Understand) Dec 2011,NOV 2016**
5. Describe the basic principle of operation of dynamic CMOS, Domino and NP Domino logic with neat diagrams. **(Understand) Dec 2011,NOV 2017**
6. Give a brief note on pass transistor logic. **(Understand)**
7. Implement XOR gate using transmission gate. **(Apply) May 2015**
8. Write short notes on **(Understand)**

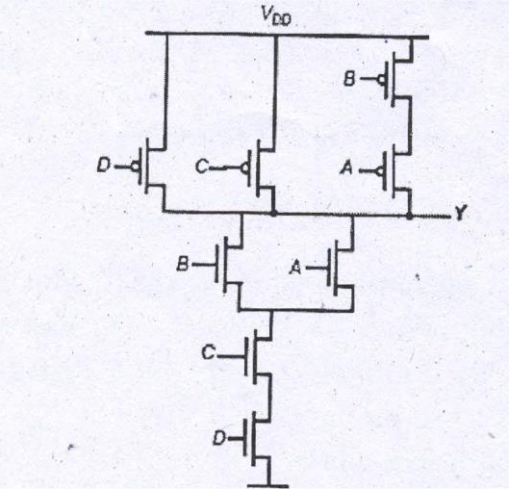
(i)Logical Effort
(ii)Delay Estimation **Dec 2012**

9. Write the basic principle of low power logic design. **(Understand) Dec 2011,Nov 2017**
10. Enumerate the features of static CMOS logic. **(Understand)**

11. Explain the characteristics of DCVSL. **(Understand) May 2017**

12. What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS? **(Analyze) May 2017, May 2016**

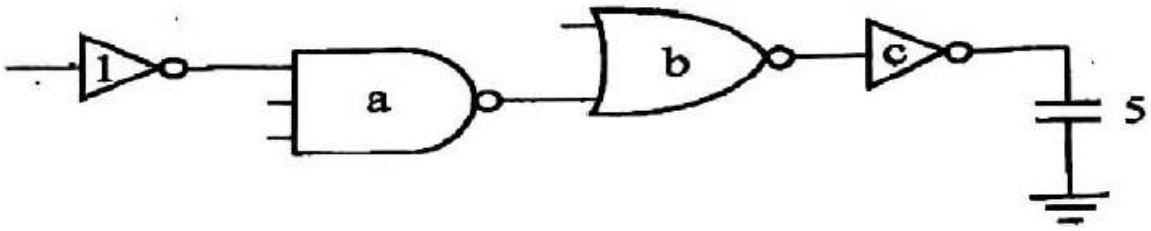
13. Consider the circuit below **(Analyze) May 2016**



(1)What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L=4 and PMOS W/L=8.
(2)What are the input patterns that give the worst case t_{pHL} and t_{pLH}.State clearly what are the initial input patterns and which input's has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.
(3)Determine the dynamic power dissipation in the logic gate.assume V_{DD} =2.5 V,C_{out} =30fF and fclk=250 MHZ.

14. Show that the output logic level of pseudo NMOS logic is independent on the size of the transistor. **(Apply) May 2016**
15. Write short notes on**(Understand) Nov 2016**
(i)Ratioed Circuits
(ii)Dynamic CMOS Circuits.
16. Briefly discuss the signal integrity issues in dynamic design. **(Understand) May 2018**

17. Obtain the logical effort and path efforts of the given circuit**. (Apply) May 2018**



18. Design a CMOS logic Circuit for the given expression y=[(A+B)(C+D)]' and draw the stick diagram**. (Apply) May 2018**

19. Design a four bit NAND gate and find its delay during the transition fron high to low **. (Apply)May 2018**

20. Draw the CMOS logic circuit for the Boolean expression Z=[(a(b+c)+de)]' and explain **(Apply)Nov 2017**

21.Implement the equation X= (A+B)CD using complementary CMOS logic. **Nov/Dec 2018 (Apply)**

(1)Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L=4 and PMOS W/L=8.

(2)What are the input patterns that give the worst case t_{PHL} and t_{PLH}. Consider the effect of the capacitance at the internal nodes.

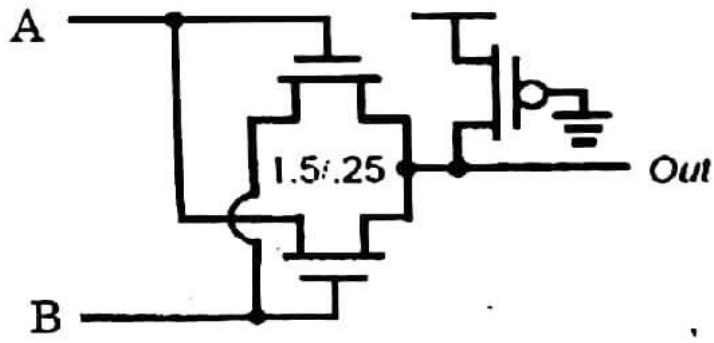
(3)If P(A=1)=0.5,P(B=1)=0.2 ,P(C=1)=0.3,P(D=1)=1,determine the power dissipation in the logic gate. Assume V_{DD}=2.5V,C_{out}=30fF and F $_{clk}$=250MHZ

22.List out the limitations of pass transistor logic. Explain any two techniques used to overcome the drawback of pass transistor logic design. **Nov/Dec 2018(Understand)**

23.Explain in detail the signal integrity issues in dynamic logic design. propose any two solutions to overcome it. **Nov/Dec 2018 (Understand)**

24.(1)Determine the truth table for the circuit shown figure-3.What logic function does it implement?

(2)If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose? **Nov/Dec 2018 (Apply)**



25. (i) Derive an expression for dynamic power dissipation. **April/May 2019 (Apply)**

(ii)Realize the following function Y = (A+BC) D+E using static CMOS logic. **April/May 2019 (Apply)**

26. Let A, B, C and D be the inputs of a data selector and S0 and S1 be the select lines. Realize a 4:1 data selector using (i) nMOS pass transistor and (ii) Transmission gate approach. Compare the hardware complexity. **April/May 2019 (Apply)**

27.Realize a 2 input XOR using static CMOS, transmission gate and dynamic CMOS logic. **(Analyze) April/May 2019.**

28.Compare the circuit implementation of 2 input multiplexer using static CMOS, domino and dual rail domino logic. **(Analyze) Nov/Dec 2021**

29.Describe the dynamic voltage scaling can reduce dynamic power dissipation. **(Analyze) Nov/Dec 2021**

30.Sketch a combinational function Y = (A(B+C+D)+ E.F.G)′ using i. Pseudo-nMOS logic ii. Domino logic iii. Cascode voltage switch logic. **(Understand)April/May 2020**

31.Explain the pass transistor logic and show how complementary pass transistor logic and double pass transistor logic are applied for 2: 1 multiplexer. **(Understand) April/May 2020**

32. Generate the partial products using radix-4 booth encoded multiplier to compute 011102 x 011012. For the same multiplier apply radix-8 booth encoding and justify the advantages between radix-4 and radix-8 booth multiplier. **(Understand) April/May 2020**

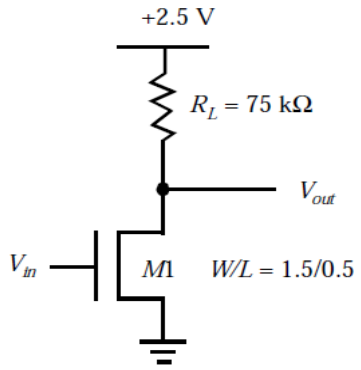
Assignment Questions:

1. For the inverter of given Figure and an output load of 3 pF:

a. Calculate *tplh*, *tphl*, and *tp*.

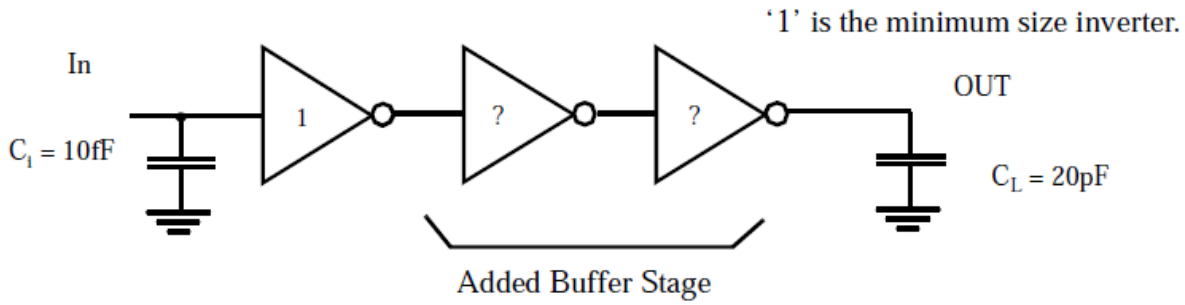
b. Are the rising and falling delays equal? Why or why not?

c. Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible. **(Apply)**



2. Sizing a chain of inverters. **(Apply)**

a. In order to drive a large capacitance (CL = 20 pF) from a minimum size gate (with input capacitance Ci = 10fF), you decide to introduce a two-staged buffer as shown in Figure. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.



3. Given the choice between NOR or NAND logic, which one would you prefer for implementation in pseudo-NMOS? **(Analyze)**

4. For the 4-input dynamic NAND gate, compute the activity factor with the following assumption for the inputs. Assume that the inputs are independent and $pA=1 = 0.2$, $pB=1 = 0.3$, $pC=1 =0.5$, and $pD=1 = 0.4$. **(Apply)**

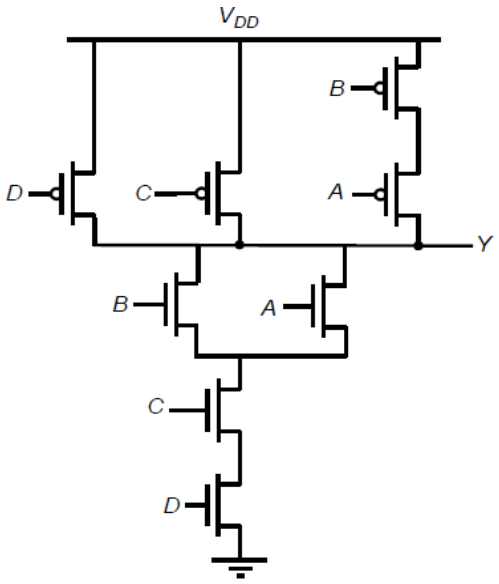
5. Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors: **(Apply)**

Y ' = □A □□B□□+ □A □□C □□E□□+ □D □□E□□+ □D □□C □□B□

6. Consider the circuit of Figure given below.

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS
and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS *W/L* = 4 and PMOS *W/L* = 8.

b. What are the input patterns that give the worst case *tpHL* and *tpLH*. State clearly what are the
Initial input patterns and which input(s) has to make a transition in order to achieve this Maximum propagation delay. Consider the effect of the capacitances at the internal nodes**.(Analyze)**



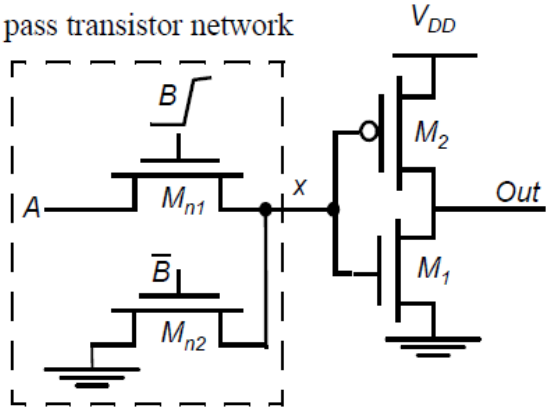
7. Consider the circuit of Figure given below. Assume the inverter switches ideally at VDD/2, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem**.(Analyze)**

a. What is the logic function performed by this circuit?

b. Explain why this circuit has non-zero static dissipation.

c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d. Implement the same circuit using transmission gates.



$V_{DD} = 2.5V$

$(W/L)_2 = 1.5um/0.25um$

$(W/L)_1 = 0.5um/0.25um$

$(W/L)_{ni} = 0.5um/0.25um$

$k_n' = 115uA/V^2$, $kp' = -30uA/V^2$

$V_{tN} = 0.43V$, $V_{tP} = -0.4V$

UNIT III SEQUENTIAL LOGIC CIRCUITS

Static latches and Registers Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. Timing Issues: Timing Classification of Digital System, Synchronous Design.

PART-A

1. Define sequential circuits. (Remember)

A sequential circuit is an interconnection of flip-flops and gates. The gates by themselves constitute a combinational circuit, but when included with the flip flops, the overall circuit is classified as a sequential circuit.

2. Define interface. (Remember)

The word interface refers to the boundary between two circuits or devices.

3. Define pipelining. (Remember) NOV 2016, May 2017

Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

4. Define parallel processing. (Remember)

Parallel processing is a term used to denote a large class of techniques that are used to provide simultaneous data-processing tasks for the purpose of increasing the computational speed of a computer system. Instead of processing each instruction sequentially as in a conventional computer, a parallel processing system is able to perform concurrent data processing to achieve faster execution time.

5. What are the components of memory management unit? (Remember)

1. A facility for dynamic storage relocation that maps logical memory references into physical memory addresses.
2 A provision for sharing common programs stored in memory by different users .
3. Protection of information against unauthorized access between users and preventing users from changing operating system functions.

6. What is programmed I/O? (Remember)

Data transfer to and from peripherals may be handled using this mode. Programmed I/O operations are the result of I/O instructions written in the computer program.

7. What is latch? (Remember)

A latch is a level sensitive circuit that passes the D input to the Q output when the clock signal is high.

8. What is register? (Remember)

Registers is a edge triggering device which samples the input only on the clock transition . Depending on the transition it may positive edge triggered register and negative edge triggered register.

9. What are the different types of latches and registers.? (Remember)

There are two different types of registers and latches .They are
(i)Static Latches and Registers.
(ii)Dynamic Latches and Registers.

10. What is clock skew? (Remember) May 2018

The spatial variation in the arrival clock is called clock skew. Clock skew may be positive and negative.

11. What are the timing issues in digital circuits? (Remember)

The two timing issues in digital circuits are clock skew and clock jitter.

12. What is the advantage of TSPC register? (Understand)

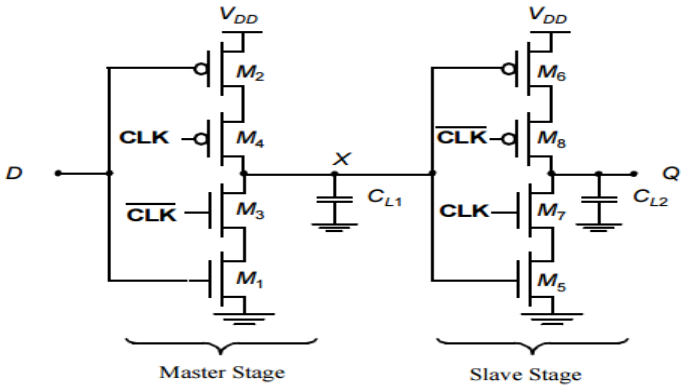
The advantage of the true single phase clocked register(TSPCR) is the use of single phase clock. Hence it avoids the overlapping problem due to clocks. The TSPC also offers the possibility of embedding logic functionality into the latches.

13. What is dual edge registers? (Remember)

The dual edge registers are designed to sample the input on both edges (rising or falling) of the clock. The advantage of this scheme is that a lower clock frequency half the original rate is distributed for the same functional throughput, resulting in power savings in the clock distribution network.

14.What is clocked CMOS register? (Remember) May 2016

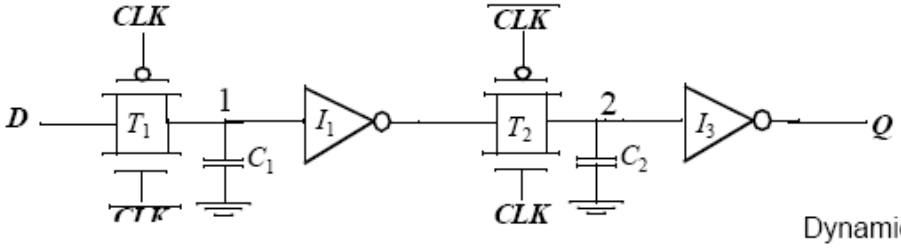
The C^2MOS register is a master slave edge triggered register which is insensitive to clock..



15. Difference between latch and Flip Flop (Understand)May 2016,May 2018 May 2020

Flip-flop	Latch
A flip-flop samples the inputs only at a clock event (rising edge, etc.)	A Latch samples the inputs continuously whenever it is enabled, that is, only when the enable signal is on. (or otherwise, it would be a wire, not a latch).
A flip-flop continuously checks its input and correspondingly changes its output only at times determined by clocking signal.	Latch is a device which continuously checks all its input and correspondingly changes its output, independent of the time determined by clocking signal.
It is an edge trigerred, it mean that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.	It is a level trigerred , it mean that the output of present state and input of the next state depends on th level that is binary input 1 or 0.

16.Draw the schematic of dynamic edge-triggered register. (Remember) Nov 2016



Dynamic *edge-triggered* register.

17.Compare and contrast synchronous and asynchronous design. (Understand)May 2017

Synchronous Design	Asynchronous Design

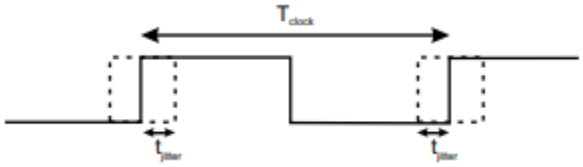
Synchronous design do not use clock and the output can change state immediately	Asynchronous design use clock and the output Change their state only when clock arrives.
Suffer from Race Conditions and intermediate states.	Do not Suffer from Race Conditions and Intermediate states.

18. What is NORA CMOS? *(*Remember) NOV 2017

A NORA data path consists of a chain of alternating CLK and CLK modules. While one class of modules is precharging with its output latch in hold mode, preserving the previous output value, the other class is evaluating. Data is passed in a pipelined fashion from module to module. NORA offers designers a wide range of design choices. Dynamic and static logic can be mixed freely, and both CLKp and CLKn dynamic blocks can be used in cascaded or in pipelined form. With this freedom of design, extra inverter stages, as required in DOMINO-CMOS, are most often avoided.

19. Define clock Jitter? *(*Remember) NOV 2017

The decrease or increase in clock period on a cycle - by- cycle basis is called clock jitter. It refers to the temporal variation of the clock period. The clock jitter is show in Fig



20. List out the advantages and limitations of 3 T DRAM over 1T DRAM. **NOV2018 (Understand)**

Advantages:

1T DRAM:

The **advantage** of a **DRAM** is the simplicity of the cell - it only requires a single transistor compared to around six in a typical static RAM, SRAM memory cell.

3 T DRAM:

In this cell, the storage capacitance is the gate capacitance of the readout device, so making this scheme attractive for embedded memory applications; however, a 3T DRAM shows still limited performance and low retention time to severely limit its use in advanced integrated circuits.

3T DRAM utilizes gate of the transistor and a capacitance to store the data value.

Disadvantages:

It is comparatively slower than SRAM. Hence **it** takes more time for accessing data or information.

It loses data when power is OFF.

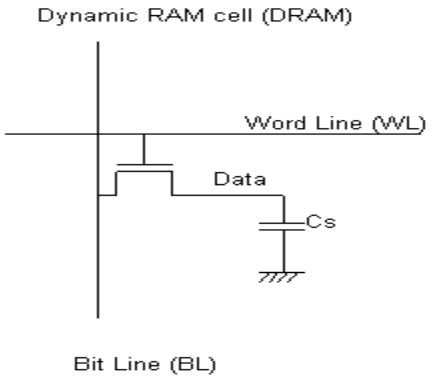
It has higher power consumption compare to SRAM.

22. Define clock skew. (Remember) April/May 2019

Clock skew (sometimes called timing **skew**) is a phenomenon in synchronous digital circuit systems (such as computer systems) in which the same sourced **clock** signal arrives at different components at different times. The instantaneous difference between the readings of any

two **clocks** is called their **skew**.

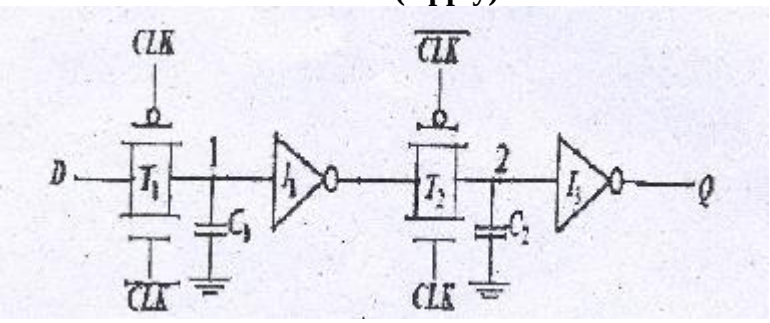
23. Draw a 1 –transistor Dynamic RAM cell.



PART-B

1. Discuss in detail various latches and registers**. (Understand)** **Nov 2016**
2. Implement and explain the Master-Slave edge triggered registers. (Apply) **May 2016,May 2018**
3. Write short notes on**(Understand)** **Nov 2016**
   (i) True single phase clocked registers. **May 2017**
   (ii)NORA-CMOS Latches
4. Explain pipelining with an example and its various approaches to optimize sequential circuits. **(Apply)** **May 2016,May2017.**
5. Discuss in detail about the timing issues in digital circuits. **(Analyze)** **May 2017**
6. Give in detail about the various sources of clock skew and clock jitter. **(Analyze)**
7. Explain the different methods of clocking scheme. **(Understand)**
8. Discuss in detail about Memory architecture .**(Analyze)**
9. Explain the Memory architecture and its control circuits**(Understand)** **May 2018**

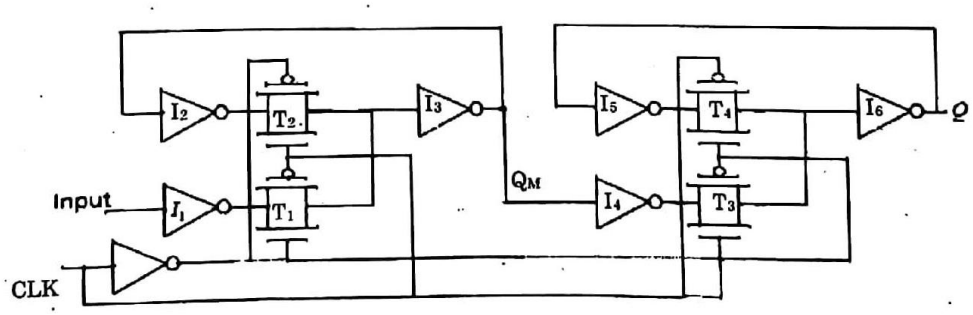
10. Explain Low power memory circuits.**(Understand**)
11. Discuss in detail about synchronous and asynchronous design**. (Analyze)**
12. Design a D latch using transmission gate. **(Create)**
13. Consider the circuit below **(Apply)**



(1)State whether the circuit is a latch or edge triggered register.Justify your answer.
(2)In the circuit consider C1 and C2 as the intrinsic capacitances of inverters and transmission gates. Assuming ideal clock, compute the setup time, hold time and propagation delay in terms of the inverter I1,I2 delay and transmission gate T1,T2 delay. **May 2016**

14.List out the issues in present in Dynamic Logic Design and Explain. **(Analyze)May2016**
15.Explain the timing basics and clock distribution techniques in synchronous design in detail.*(***Understand)** **Nov 2017**

21. Discuss about the design of sequential dynamic circuits and its pipelining Concept**.(Understand***)* **Nov 2017**
22.(a)(i) Identify the type of register for the circuit shown in figure 4 and express setup time, hold time and propagation delay register in terms of the propagation delay of inverters and transmission gates. **(Apply) Nov 2018**



(ii) Implement the register of question13 (i) using C2MOS logic and explain how 0-0 and 1-1 overlap of clock signals are eliminated. **(Apply) Nov 2018**
23. (i) construct 6T based SRAM cell. Explain its read and write operations. What is the importance of cell ratio and pull up ratio in 6T SRAM cell? **(Apply) Nov 2018**
(ii)Analyze the impact of spatial variations of clock signal on edge triggered sequential logic circuits. **(Analyze) Nov 2018**
24. Design a D-Latch using Transmission gate. Using which realize a two phase non overlapping master-slave negative edge triggered D-Filp- flop. **(Design)April/May 2019**
25. Elucidate in detail low power SRAM circuit. (**Understanding) April/May 2019**
26.Explain the circuit and working of working of CMOS implementation of Schmitt Trigger. **(Analyze)Nov/Dec 2021**
27.Discuss the timing parameter that characterize the timing of sequential circuit. **(Anayze)Nov/Dec 2021**
28.Ellaborate on rotate right and rotate left operation using barrel shifters. **(Analyze)Nov/Dec 2021**
29.Draw the NOR and NAND implementation of word,4bit ROM. **(Analyze)Nov/Dec 2021**
30.a) i. Illustrate the circuit designs for basic latches, then build the flip-flops and pulsed latches.
ii. Design the pulse registers suitable for sequential CMOS circuits. (**Understanding) April/May 2020**
31.b) i) Describe the concept of pipelining in sequential circuits with a suitable example.
ii) Sketch and explain the Monostable sequential circuits based on CMOS logic.
(**Understanding) April/May 2020**

Assignment Questions:

1. Explain the Bi-stability principles in static latches and registers**.(Understand)**

2. Explain positive edge triggered register based on sense amplifier. **.(Understand)**
3. Design a 1-transistor DRAM cell**.(Create)**
4.Draw the circuit diagram of 6T SRAM cell and explain it's working**.(Understand)**
5.Discuss in detail about synchronous and asynchronous design**. (Analyze)**
6.Give in detail about the various sources of clock skew and clock jitter. **(Analyze)**

UNIT IV DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff. Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

Part – A

1.What is bit slicing?(Remember) **May 2016**

Bit slicing is a method of constructing a processor from modules of single bit width to full word length. For eg. 32 – bit processor operates on data words that are 32 – bits wide. Since the same operation has to be performed on each data bit, the data path consist of 32 – bit slices, each operating on a single bit.

2. What are the methods used for optimizing the adder? (Remember)

The adder can be optimized in two levels

(i) Logic Level – Rearrangement of Boolean equation to speed up the circuits
(ii) Circuit Level – The transistor size and the circuit topology is manipulated to decrease the area and power.

3. What is meant by generate propagate and delete? (Remember)

G-Generate, D-Delete, P-Propagate are the intermediate signals of adder.

When G=1, then the output carry will be generated i.e., $C_0 = 1$ irrespective of C_i
When D=1, then the output carry will be Deleted i.e., $C_0 = 0$ irrespective of C_i
When P=1, then the output carry will be Propagates same as C_i i.e., $C_0 = C_i$
$G=AB \quad \bar{D}=\bar{A}\,\bar{B} \quad p=A \oplus B$.

4. What is the worst case delay of the ripple carry adder? (Remember)

In certain input patterns, the carry will ripple all the way from the least significant bit(LSB) to the most significant bit(MSB). The propagation delay of such case is called worst case delay.

5. What is called Manchester- carry-chain adder? (Remember)

A Manchester- carry-chain adder uses a cascade of pass transistors to implement the carry-chain.

6.Give the propagation delay of N-bit ripple carry adder?

The propagation delay of the ripple carry adder is linearly proportional to N-bit.

$t_{adder}=(N-1)\ t_{carry} + t_{sum}$

7. What is partial product generation? (Remember)

Partial product results from the multiplication of the multiplicand X with the multiplier bit y_i i.e., it is an AND operation of two bits. Each row in the partial product array is either a copy of the multiplicand or row of zeros depending on y_i

8. What is called booth recoding? (Remember)

Consider a eight bit multiplier number 0111 1110, which produces six non-zero partial product rows. The number of non-zero rows can be reduced by recoding this number. In Booth, recoding the multiplier bit is divided into 2 bit groups and overlapped by 1 bit.

Eg: 0111 1110 ⟶ 100000-10

Booth recoding.

9.How carry save multiplier differs from array multiplier? (Understand)

In carry save multiplier, the output carry bits are passed diagonally downwards instead of passing right. This results in shortest critical path but an extra adder is needed comparing to array multiplier.

10.Why the partial sum adders are arranged in tree like fashion? (Understand)

The partial sum adders are arranged in a tree like fashion to reduce both the critical path and the number of adder cells needed.

11.Difference between ripple carry adder and carry select adder? (Understand)

In ripple carry adder, the full adder cell has to wait for the incoming carry before an outgoing can be generated. The propagation delay is proportional to N (linearly).

But in carry select adder the output carry is evaluated for both the possibilities of input carry and then selected afterwards. The propagation delay is proportional to $\sqrt{N}$.

12.Give the booths recoding transformation of the following number (Apply)

0 1 1 1 1 0 0 1 (0)

1 0 0 0 -1-0 1 -1 ⟶ Booth's recoding

13.Give the difference between Booth's recoding and modified Booth's recoding? (Understand)

Booth's recoding:

In Booth's recoding, the multiplier is partitioned into two bit groups and overlap by one bit.

Modified Booth's recoding:

In modified Booth's recoding, the multiplier is partitioned into three bit groups and overlap by one bit.

14. Determine propagation delay of n-Bit carry select adder.(Remember) **May 2016**

The propagation delay of n-Bit carry select adder.

$$t_p = t_{setup} + M\,t_{carry} + \left(\frac{N}{M}\right) t_{mux} + t_{sum}$$

Where

t_{setup} → time taken to compute generate and Propagate signals
t_{sum} → time taken to compute sum
t_{mux} → delay in the multiplexer
t_{carry} → delay of the carry path of a single bit
N → No of bits
M → No of bits/stage

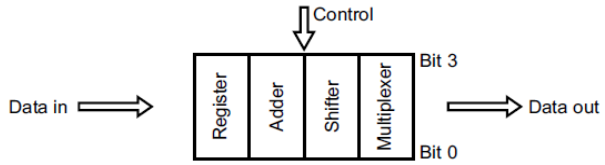
15.Give the application of high speed adder.(Remember) **May 2017**

The fast adders are needed in larger structures such as multipliers or high speed signal processors. Some adders that are fast is

1. Kogge - Stone Look ahead Logarithmic Adder
2. Carry Save Adder.

16.List out the components of datapath. .(Remember) **May 2017**

The data path is the core of the processor. A data path consists of arithmetic logic unit & Shifters to perform data processing operations, registers and buses. More buses are used to transfer the data between components.



Bit-sliced datapath organization

17. Write the principle of any on fast multiplier.(Understand) **Nov 2016**

To implement faster multiplier, all the partial products are generated at the same time and organized in an array. Finally, addition is applied to compute the final product. This resulting structure is called array multiplier.

Multiplier consists of three functions

1. Partial Product generation
2. Partial Product Accumulation
3. Final Addition

18.Why barrel shifter is very useful in the arithmetic circuits? (understand) Nov 2016

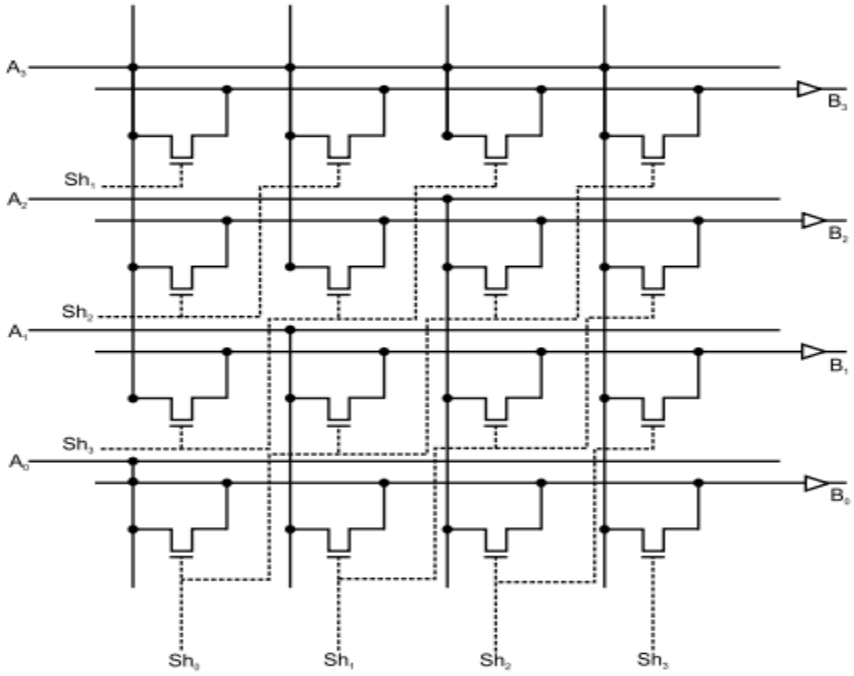
A barrel shifter is a circuit that can shift a data word by a specified number of times in one clock cycle. It consists of an array of transistors. The barrel shifter has a variety of applications, including being a useful component in microprocessors (alongside the ALU).A common usage of a barrel shifter is in the hardware implementation of floating-point .

19. Write the full adder output in terms of propagate and generate.(Remember) May 2018

Cout = G + PCin

Sum= P ⊕ Cin

20.Draw the structure of 4*4 barrel shifter. .(Remember) May 2018



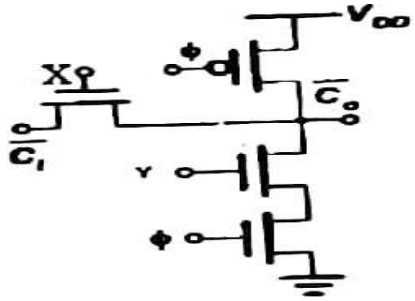
21. How to design a high speed adder? .(Remember) Nov 2017

The fast adders are needed in larger structures such as multipliers or high speed signal processors. The high speed adder can be designed by reducing the time delay for the generation of carry.

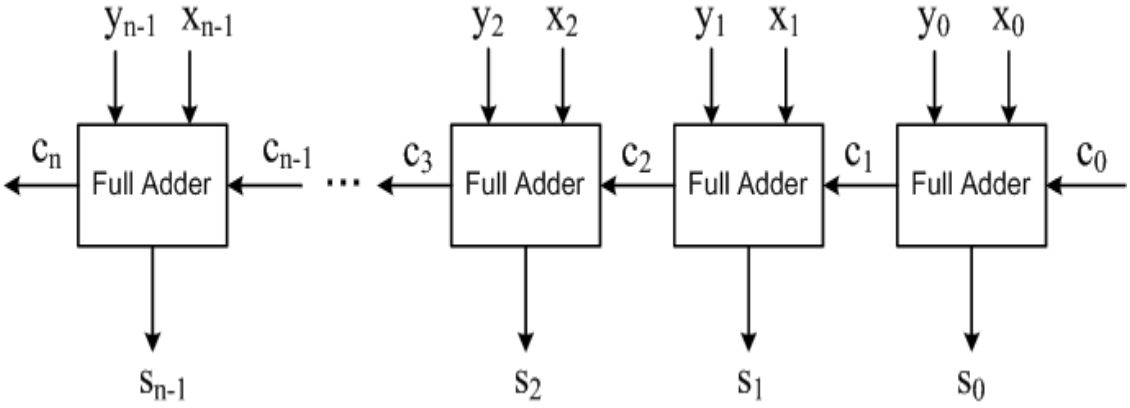
22. What is latency? .(Remember) Nov 2017

The performance of the system is increased with pipelined system. But the latency i.e. the number of clock cycles required to get the output increases.

23.The circuit in figure.2 shows a carry propagation path in adder in an adder circuit. Let A,B,Ci are the inputs to adder circuit and ψ is the clock signal. Write the logic expressions for the signal X,Y to generate output carry. **(Analyze) NOV2018**



24. Draw a 4 bit ripple carry adder and find its critical path delay **(Understand) Nov 2018**



25. Define kill term, propagate and generate term in a carry look ahead adder. **(Remember)April/May 2019**

G-generate D-delete and P-propagate are the intermediate signals of adder.
When G=1,then the output carry will be generated i.e C_0=1 irrespective of C_i
D=1 ,then the output carry is deleted i.e C0=0 irrespective of Ci
When P=1,the output carry is propagated same as C0 i.e C0=Ci
G=AB,D=AB P=A+B

26. State radix-2 booth encoding table. **(Remember)April/May 2019**

Multiplier bits	**Recoded bits**		**Comments**
Xi	**X_{i-1}**	**Y_i**	
0	**0**	**0**	**Shift only**
0	**1**	**0**	**Shift add**
1	**0**	**-1**	**Shift Subtract**
1	**1**	**0**	**Shift only**

Part - B

1. Draw and explain the transmission gate based adder? **(Understand)**
2. Explain the operation of a basic 4 bit adder; Describe the different approaches of improving the speed of the adder. **(Understand) Nov 2016**
3. Explain logarithmic look ahead adder with necessary block generates and propagate signal. **(Understand) May2017,May 2018**
4. Explain the operation of a booth multiplication with suitable examples? Justify how booths algorithm speed up the multiplication process. **(Understand) Nov 2016**
5. Draw the 4 bit array multiplier and explain in detail. **(Understand) May 2016**
6. Explain about the barrel shifter. **(Understand)**
7. Explain about the division concept and draw its structure. **(Understand)**
8. Draw and explain the implementation of full adder using Manchester carry chain adder. **(Understand)**
9. Explain any two types of High Speed Adder. **(Understand)**
10. Design a 16 bit carry bypass and carry select adder and discuss their features. **May 2016(Analyze)**
11. Discuss the details about speed and tradeoff**. (Analyze) May 2017**
12. Explain the concept modified booth algorithm with an example**. (Understand)May 2017**
13. Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. **(APPLY)Nov 2017**

14.Draw the structure of ripple carry adder and explain its operation. How the drawback in ripple carry adder overcome by carry look ahead adder and discuss**.(Analyze) Nov 2017**

15. Design an 8 bit Brent kung adder. **(Design) Nov 2018**
16. Construct4*4 array type multiplier and find its critical path delay. **(Create) Nov2018**
17. Design 4-input and 4-output barrel shift adder using NMOS logic **(Design) Nov 2018**
18. Derive the necessary expression of a 4 bit carry look ahead adder and realize the carry out expression using Dynamic CMOS logic. **(Apply) April/May 2019**
19. Design a 4-bit unsigned array multiplier and analyze its hardware complexity. **(Apply) April/May 2019**
20. Apply radix-2 booth encoding to realize a 4 bit signed multiplier for (-10)*(-11). **(Apply) April/May 2019**

21a) i) Explain the carry-propagate adder and show how the generation and propagation signals are framed. ii) List the several commonly used shifters. Design the shifter that can perform all the commonly used shifters. **(Understand) April/May 2020**

22. Illustrate the building blocks of Memory architectures and memory peripheral circuitry adapted to operate for non-volatile memory. **(Understand) April/May 2020**

Assignment Questions:

1.Design the arithmetic logic unit (ALU) of 16 bits. (**Create)**
2.Give a short note on Logarithmic shifter. **(Understand)**
3. Compare the advantages of Carry bypass adder compared to other adders**.(Analyze)**
4. Explain the inverting property of full adder. **(Understand)**
5. Explain 4 bit Kogge Stone Adder. **(Understand)**
6. Design a 4 bit carry bypass adder and verify with Xilinx tool.(**Create)**

7.Explain about the Booth's recoding and modified Booth's recoding. **(Understand)**

UNIT V IMPLEMENTATION STRATEGIES AND TESTING

FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

PART-A

1. Write the design style classification? (Remember)

The IC design style can be classified as

(1) Full custom Design ASICs

(2) Semi-custom Design ASICs
- (a) Standard Cell Design
- (b) Gate Array Design
  - (i) Channeled Gate Array
  - (ii) Channel less Gate Array

(3) Programmable ASICs
- (a) PLDs
- (b) FPGA

2. What are the two types of ASICs? (Remember)

Types of ASICs are
Full custom ASICs
Semi-custom ASICs

3. What are the types of programmable devices? (Remember)

Types of programmable devices are
(1) Programmable Logic Structure

(2) Programmable Interconnect.
(3) Reprogrammable Gate Array.

4. What are the different types of programming structure available in PAL? (Remember)

Programming Techniques of PAL are
(1) Fusible links programming

(2) UV-Erasable EPROM programming
(3) EEPROM programming

5. Why CMOS technology is most useful for analog functions? (Understand)

The first reason is that CMOS is now by far the most widely available IC technology. Most CMOS Asics and CMOS standard products are now being manufactured than bipolar ICs. The second reason is that increased levels of integration require mixing analog and digital functions on the same IC: this has forced designers to find ways to use CMOS technology to implement analog functions.

6. What are the features of standard celled ASICs? (Remember)

All mask layers are customized- transistors and interconnect.
Custom blocks can be embedded.
Manufacturing lead time is about eight weeks.

7.What is the difference between channeled gate array and channel less gate array? (Understand)

The key difference between a channel less gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate –array devices. We can do this because we customize the contact defines the connections between metal1, the first layer of metal and the transistors.

8. What are the characteristics of FPGA? (Remember)

- None of the mask layers are customized
- A method for programming the basic logic cells and the interconnect.
- The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops).
- A matrix of programmable interconnect surrounds the basic logic cells.
- Design turnaround is a few hours.

9. What is programmable logic array? (Remember)

A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes, which can then be conditionally complemented to produce an output an output. This layout allows for a large number of logic functions to be synthesized in the sum of products (and sometimes product of sums) canonical forms.

10. What is mean by Programmable logic plane? (Remember)

The Programmable logic plane is programmable read -only memory (PROM) array that allows the signals present on the devices pins (or the logical components of those signals) to be routed to an output logic macro cell.

11. Describe the steps in ASIC design flow? (Understand)

- Design entry. Enter the design into an ASIC design system, either using a hardware

description language (HDL) or schematic entry.
Logic synthesis. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a net list – a description of the logic cells and their connections.

- System partitioning. Divide a large system into ASIC- sized pieces.
- Pre layout simulation. Check to see if the design functions correctly.
- Floor planning. Arrange the blocks of the net list on the chip.
- Placement. Decide the locations of cells in a block.
- Routing. Make the connections between cells and blocks.
- Extraction. Determine the resistance and capacitance of the interconnect.
- Post layout simulation. Check to see the design still works with the added loads of the interconnect.

12. Give the application of PLA (Remember)

PLA is used in Design and testing of digital circuits

13. What is the full custom ASIC design? (Remember) May 2016

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

14. What is the standard cell-based ASIC design? (Remember) NOV 2017

A cell-based ASIC (CBIC) USES PREDESIGNED LOGIC CELLS KNOWN AS STANDARD CELLS. The standard cell areas also called fle4xible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

15. What is a FPGA? (Remember)

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of up to about 20,000 equivalent gates.

16. What are the different methods of programming of PALs? (Remember)

The programming of PALs is done in three main ways: Fusible links
UV – erasable EPROM
EEPROM (E 2PROM) – Electrically Erasable Programmable ROM

17. What is an antifuse? (Remember) NOV 2016

An antifuse is normally high resistance (>). On application of appropriateΩ100M

programming voltages, the antifuse is changed permanently to a low-resistance).Ωstructure (200-500

18. What are the different levels of design abstraction at physical design. (Remember)

Architectural or functional level
Register Transfer-level (RTL)
Logic level
Circuit level

19. What are macros? (Remember) 9444465002

The logic cells in a gate-array library are often called macros.

20. What are Programmable Interconnects? (Remember)

In a PAL, the device is programmed by changing the characteristics of the switching element. An alternative would be to program the routing.

21. What are the types of gate arrays in ASIC? (Remember)

1) Channeled gate arrays
2) Channel less gate arrays
3) Structured gate arrays

22. What are feed through cells? State their uses. (Remember) May 2016

The connection between the rows of standard cells is made by feed through. Feed through is a piece of metal used to pass a signal through a cell or to a space in a cell.

23. What is meant by CBIC? (Remember) May 2017
A cell based ASIC (or) cell based IC (CBIC) uses predesigned logic cells like AND gates, OR gates, Multiplexers & flip flops. These predesigned logic cells are known as **standard cells**.

24. Name the elements in the Configuration Logic Block (Remember) May 2017
The configurable Logic Blocks (CLB's) constitute the main logic resource for implementing synchronous as well as combinational circuits. Each CLB contains four slices and each slice contains two Look-up Tables(LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches.

25.What is the role of cell libraries in ASIC design .(Remember) May 2018

A typical standard - cell library contains two main components.

1. Library database -consists of a number of views often including layout, schematic, symbol, abstract, and other logical or simulation views

2. Timing Abstract - Generally it provides functional definitions, timing power and noise information for each cell. A standard - cell library may also contain the following additional components:

• A full layout of the cells
• Spice models of the cells
• Verilog models or VHDL models
• Parasitic Extraction models
• DRC rule decks.

26.What are the two different types of routing? .(Remember) Nov 2017,May 2018

Types of routing 1. Global routing 2. Detailed routing

Global routing methods:

There are two approaches in global routing 1. Sequential routing 2. Hierarchical routing

27.What is ULSI? .(Remember) Nov 2017

Ultra large-scale integration (ULSI) is the process of integrating or embedding millions of transistors on a single silicon semiconductor microchip. ULSI technology was conceived during the late 1980s when superior computer processor microchips, specifically for the Intel 8086 series, were under development. ULSI is a successor to large-scale integration (LSI) and very large-scale integration (VLSI) technologies but is in the same category as VLSI.

28. Differentiate between full custom design and semi-custom design. **(Understand)Nov2018 April/May 2019**

Full custom design requires all **the** components to be **designed** and verified right from **the** transistor level. This methodology is used for mass production and to optimize area speed and power. However **semi-custom design** are used when there is less time for **design** and for less quantities.

29. State the three important blocks in FPGA architecture. (Understand)April/May 2019

They are I/O **blocks** or Pads, Switch Matrix/ Interconnection Wires and Configurable logic **blocks** (CLB). The basic **FPGA architecture** has two dimensional arrays of logic **blocks** with a means for a user to arrange the interconnection between the logic **blocks**.

30. What is the aim of adhoc test techniques? (Remember)Nov2021

The collections of various test methods are known as Ad-hoc testing. The aim of adhoc test technique is to reduce the combinational explosion of testing. The common techniques for ad-hoc testing are

- Partitioning large sequential circuits.
- Adding test points
- Adding multiplexers
- Providing for easy state reset.

31. Distinguish functionality test and manufacturing test? (Understanding)

S.No	Functionality Test	Manufacturing Test
1.	It is used to verify the functionality of the circuit	It is used to verify the function of gate and register in the chip.
2.	It is used to prove that, the circuit is functionally equivalent to some specification.This specification may be VHDL or Verilog.	It is necessary, because during the manufacturing process, the chip may be experienced by over voltage and over temperature process

32. What is the need for testing? (Remember)

IC fabrication is very complex process.So, there may be any imperfection occur in any one of the stage. The imperfection may affect the result, So testing is necessary to find out which IC is good and which IC is bad.

33. What is fault coverage? (Remember)

A measure of goodness of a set of test vectors is the amount of fault coverage it achieves.The fault coverage of a set of test vectors is the percentage of total nodes that can be detected as faulty when the vectors are applied.

34. What are the advantages and disadvantages of BIST? (Remember)

Advantages:

- Testing may be completed when the part is in the field. It reduces the time required.
- It can reduce the overall system cost
- With care, self-test can be performed during normal system operation.

Disadvantages:

- It adds area to the chip for test logic.

35. What is IDDQ testing? [MAY '2011] (Remember)

A method for testing bridging faults is called IDDQ testing. It is based on the assumption that, the variation in the current reading indicates that there is problem in the chip. When the cmos logic gate is not switching, it draws no DC current, but if there is fault the a small DC current flows.

36. What is memory self-test? (Remember)

Testing large memories with a production tester is expensive because they have more no of bits. So self-test circuits are embedded within the memories and it reduces

37. Give the different approaches in design for testability/classification of testing? [MAY '2013] (Remember)

There are three main approaches in design for testability

- Ad-hoc testing.
- Scan based Test
- Built-in self -test [BIST].

38. What are the major classifications of testing? (Remember)

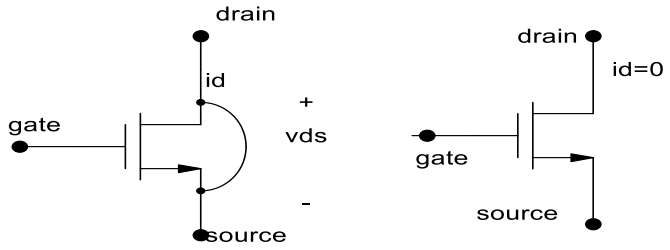
Major classification of Testing is,

(i)Functionality Tests

(ii)Manufacturing Tests

39. Draw the short circuit and open circuit model. (Remember)

Short circuit model: open circuit model:



In sc model, source is shorted with drain

In oc model, drain is opened. and id=0.

40. What is BILBO? (Remember)

BILBO means Built-in-logic Block observer. It is a combination of signature analysis and scan technique. This circuit is used to allow them to perform operations upon themselves that prove correct operation.

41. What is controllability? (Remember)

The Controllability of the node is defined as measure of case of setting the node to logic-0-state (or) logic-1-state.This metric is of importance when assessing is the degree of difficulty of testing a particular signal within a circuit.

42. What is observability? (Remember)

Observability of IC node is the degree to which we can observe that node, at the output of an IC.This metric is of importance when measuring the output of a gate within a larger circuit to check that it works correctly.

43. What is ATPG? (Remember)

Methods to generate the tests automatically are invented and are called as ATPG [Automatic Test Pattern Generation].The commercial ATPG tools can achieve excellent fault coverage.

44. Define TDR. (Remember)

TDR means Test-Data Register. They are used to set the inputs of modules to be tested and collect the results of running tests. It consists of a boundary scan register and bypass register.

45. What are the advantages of single stuck at fault? [MAY'2012] (Remember)

- Can be applied at the logic level or module level
- Reasonable numbers of faults 2n where n= number of circuit nodes
- Algorithms for automatic test pattern generation (ATPG) and fault simulation are well developed and efficient
- This covers source –drain shots ,oxide pin holes ,missing feature, diffusion contaminants, metallization short etc.

46. What are the factors that cause timing failures? [MAY'2012] (Remember)

With feature sizes shrinking, manufacturing defects and parameter variations often cause design timing failures. Cross talk coupling is one of such causes.

47. State the objective of functionality test. [NOV '2011] (Remember)

Functional tests verify the functionality of the device or circuit. Functionality tests verify for a particular input vector whether the device yield the right output or not.

48. What is text fixures? (Remember) [NOV '2011]

A socket for transmitting electrical signals from the test signal generation [IC tester] to an IC device-under –test (DUT) is called test fixures.

49. What are the advantages of LSSD? (Remember)

- The circuit operation is independent of the dynamic characteristics of the logic elements rise and fall times and propagation delays.
- ATPG is simplified since tests need only be generated for a combinational circuit
- LSSD methods ,when adopted in design ,eliminate hazards and a race greatly simplifies test generation and fault simulation.

50. What are the stages at which a chip can be tested? (Remember)NOV '2012

Testing a chip can occur at the

- Wafer level
- Packaged chip level
- Board Level
- System Level
- Field Level

51. Distinguish testers and test fixures (Remember) NOV '2012

S.No	Testers	Test Fixures
1.	A tester is a device that can apply a sequence of stimuli to a chip or system under test and monitor and record results of those operations	A socket for transmitting electrical signals from the test signal generation [IC tester] to an IC device-under –test (DUT) is called test fixtures.

PART- B

1. Explain Full custom VLSI Design flow. **(Understand) May 2016**
2. Explain the various types of ASIC design with a neat diagram **(Understand).Nov 2017, May 2018**
3. Explain Semi custom design VLSI Design flow with its classification**. (Understand) May 2016,NOV 2016,May 2017**
4. Explain Standard cell design and cell libraries. **(Understand)**
5. Discuss in detail about FPGA building block architectures**(Understand)May 2017,May 2018,Nov 2017**
6. Discuss in detail about FPGA interconnect routing procedures. **(Understand)May 2017**
7. Draw and explain the Xilinx XC4000 FPGA architecture. **(Understand) May 2016**
8. Explain the Altera FPGA architecture. **(Understand)**
9. Discuss the different types of programming technology used in FPGA design**.(Understand) NOV 2016**
10. Explain CLB of Xilinx 4000 architecture. **(Understand) NOV 2018**
11. (i)Realize the function F=A.B+(B'C)+D using ACTEL(ACT-1) FPGA**.(Apply)Nov 2018**

(ii)Draw the flow chart of digital circuit design techniques. **(Understand) Nov2018**

(iii)Differentiate between Hard Macro and Soft Macro. **(Understand) Nov 2018**

12. Elucidate in detail the basic FPGA architecture. (Understand) April/May 2019

13 .Describe FPGA interconnect routing resources with neat diagram. **(Understand)**

April/May 2019

13. Explain the system level test techniques. **(Understand)**

14. Explain the principles of silicon debug &fault models. **(Understand)**

MAY'2012, NOV '2012, [MAY '2013]

15. Explain the manufacturing test principles in detail **(Understand)** **NOV '2011**

16. Explain in detail Boundary scan test. **(Understand)** **[MAY '2013]**

17. Explain the ADHOC testing. **(Understand)** **NOV '2011**

18. Explain the terms controllability, observability and fault coverage. **(Understand)**

19. Explain in detail the sequence of Scan Based technique? **(Understand) MAY '2011, 2012 /NOV '2011**

20. Explain the principles of BIST. **(Understand)** **MAY '2011**

21. Explain how a Pseudo-random sequence generator can be used to test a 16-bit data path. How the outputs be controlled and checked **(Understand)** **MAY'2012**

22. Briefly explain about TAP controller. **(Understand)**

23. Enumerate on physical faults with examples. **(Understand)**

24. Explain in detail about partition and MUX testing **(Understand)** **MAY'2012**

25. Explain how to detect a stuck at fault with example**. (Understand)** **NOV '2012**

26. Explain the design for testability (DFT) concepts. **(Understand)** **[MAY '2013]**

27.i) Show how routing is performed in FPGA interconnect. ii) Illustrate the basic building block architectures of FPGA (Understand) April/May 2020

28. Explain the three main approaches commonly used for design for testability (DFT).

Assignment Questions:

1. Classify the types of FPGA routing techniques and explain**.(Analyze)**
2. How many global buffers are there in your current FPGA, what is their significance**? (Apply)**
3. Describe the techniques involved in Switch box programmable wiring**. (Understand)**
4. Compare two types of macro cells. **. (Understand)**
5. Difference between FPGA and CPLD. **(Analyze)**

6. Explain any one chip architecture that used the antifuse and give its advantages. **(Understand)**